Spintronics Applications At NVE

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Outline

- **NVE Corporation**
- **Angular Position Sensor**
- **Isolator - Linear Material**
- **Magneto-Thermal MRAM**

Ist Annual CNS Nanotechnology Symposium
Nanomagnetics - From Discovery To Systems

Cornell University May 14, 2004

NVE Product Lines

- Sensors
- Isolators
- Nonvolatile Memory
- Contract Research

NVE Sensors

- GMR Multilayers
- Variations Of Spin Valves
- Product Advantages
  - Size
  - Sensitivity
  - Cost

NVE Isolators

- Coil + On-Chip Sensor
- Variation Of Spin Valve
- Product Advantages
  - Speed (Compared To Optos)
  - Multi-channel (Board Space)
  - Cost Competitive

Nonvolatile Memory

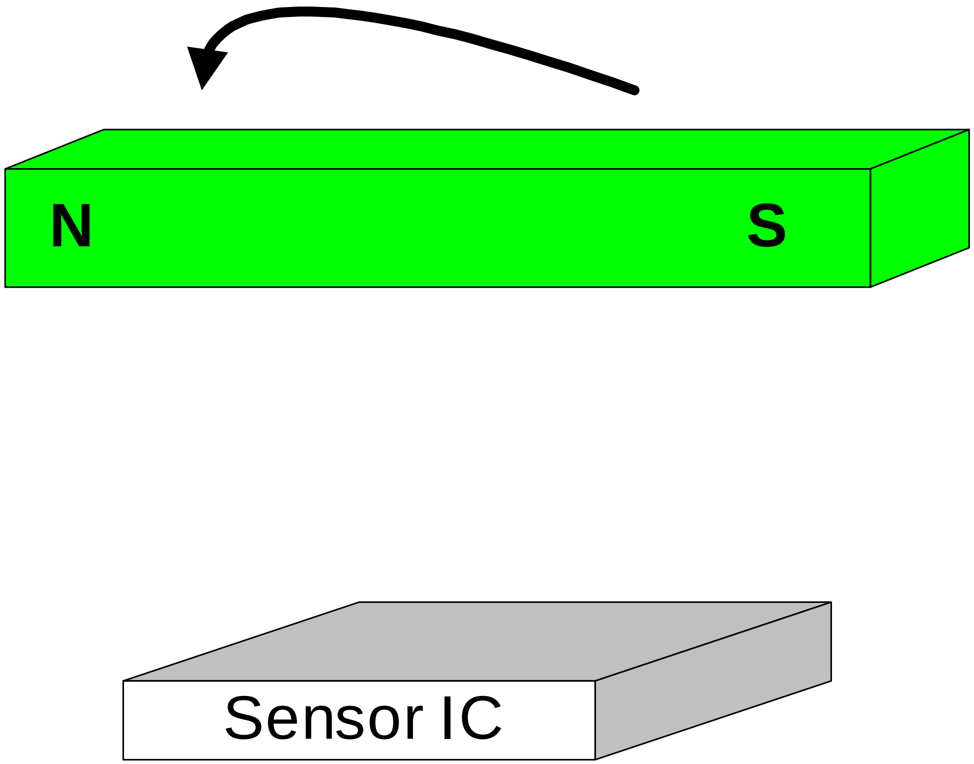
- Licensees
  - Honeywell - Other
  - Motorola
  - USTC
  - Cypress
- Potential - Niche MRAM

Metrics

- ~ 70 Employees - 12 PhDs
- ~ Annual Revenue - $12M
- ~ Annual Profit - $ 2M
- ~ $7M Cash

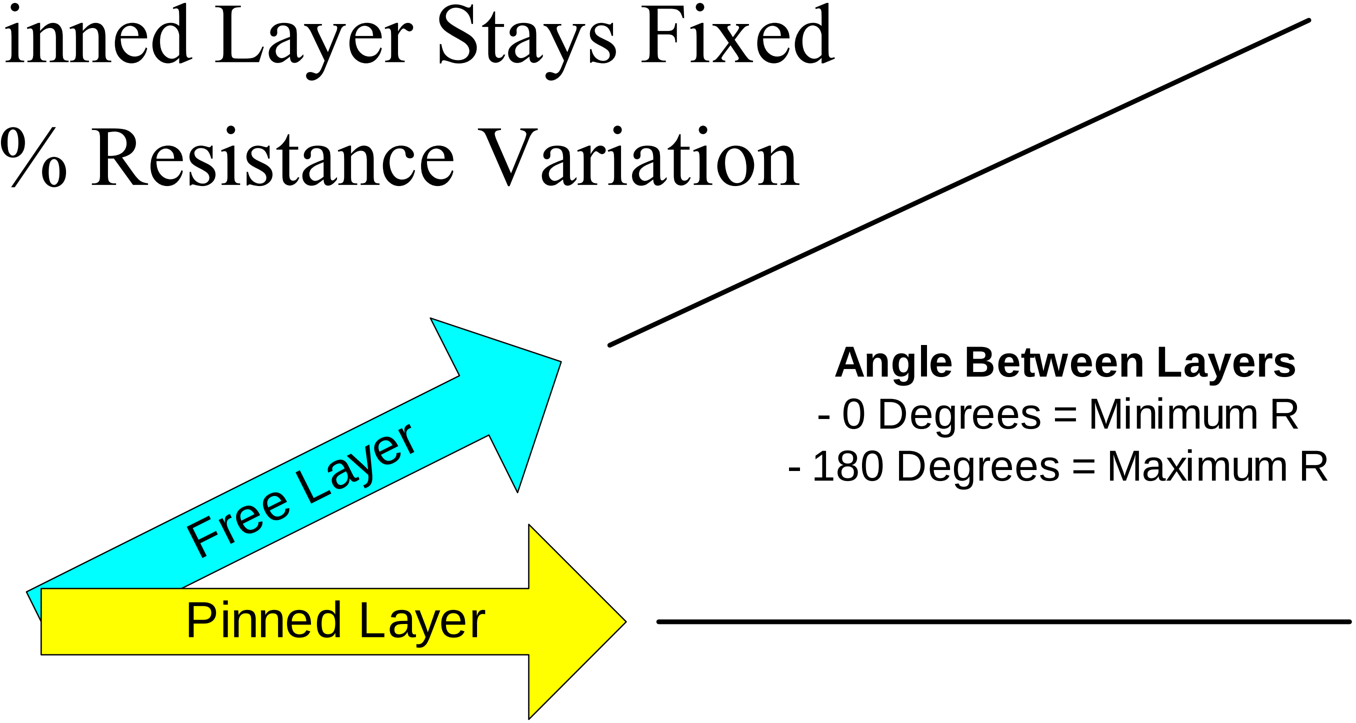
Angular Position Sensor

Rotation of Magnet Yields Output



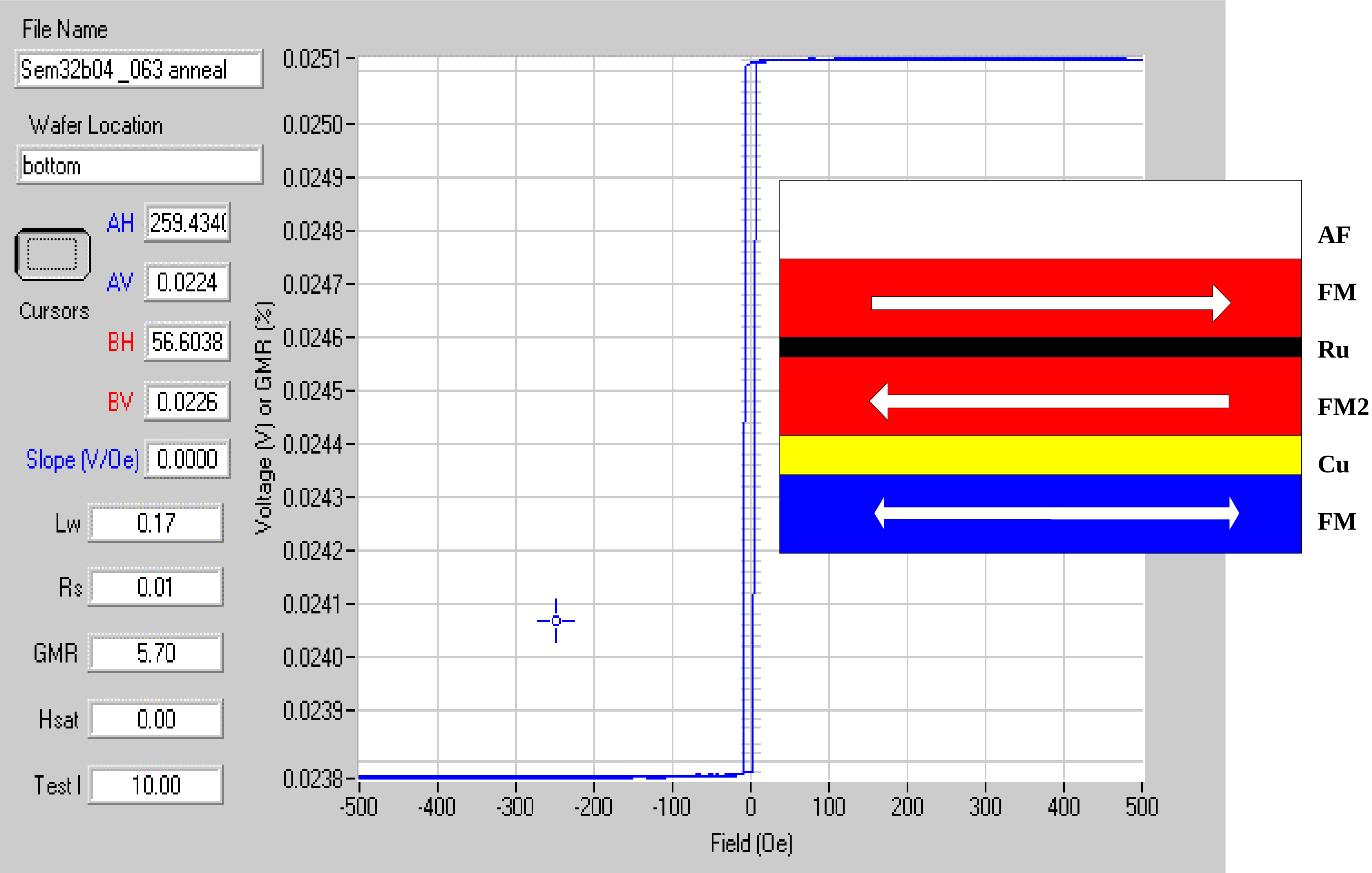
Angle Sensor GMR Spin Valve

- Operates in Saturation
- External Magnetic Field “Captures” Free Magnetic Layer in Device
- Pinned Layer Stays Fixed
- 5% Resistance Variation



Angle Between Layers
- 0 Degrees = Minimum R
- 180 Degrees = Maximum R

Spin Valve with SAF Pinned Layer



File Name: Sem32b04 _063 anneal

Wafer Location: bottom

AH: 259.434

AV: 0.0224

BH: 56.6038

BV: 0.0226

Slope (V/Oe): 0.0000

Lw: 0.17

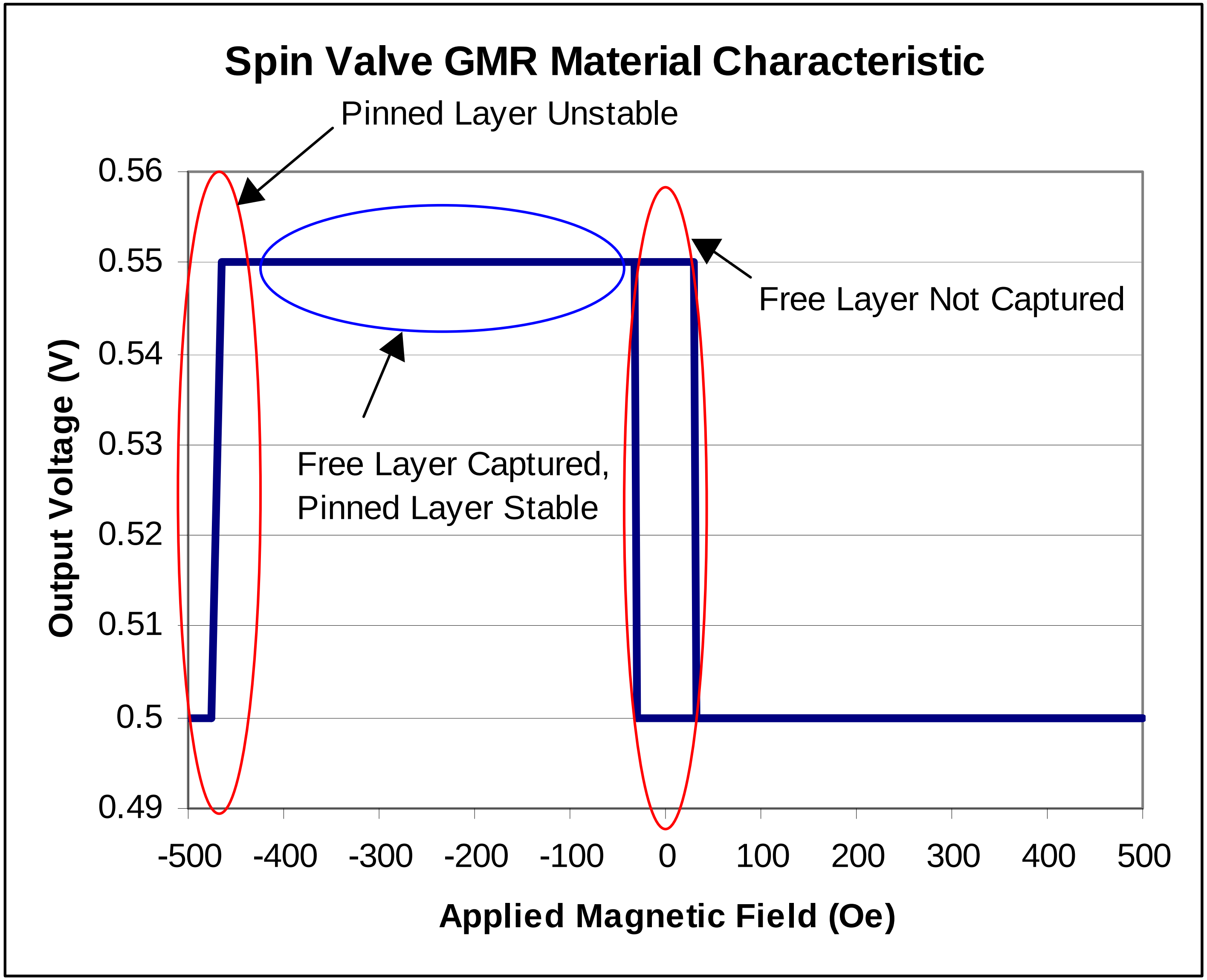
Rs: 0.01

GMR: 5.70

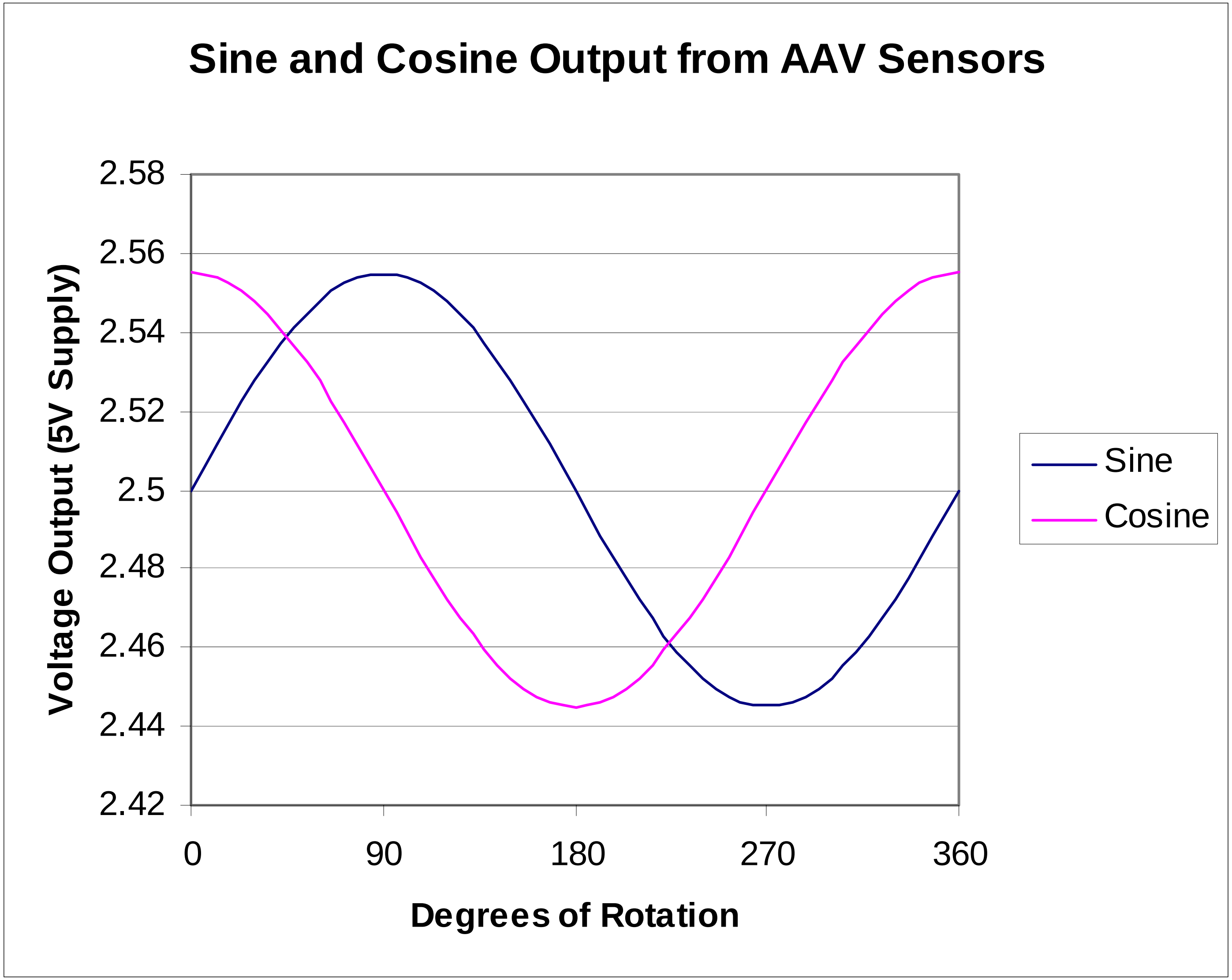
Hsat: 0.00

Test I: 10.00

Field Range of 30 to 200 Oe



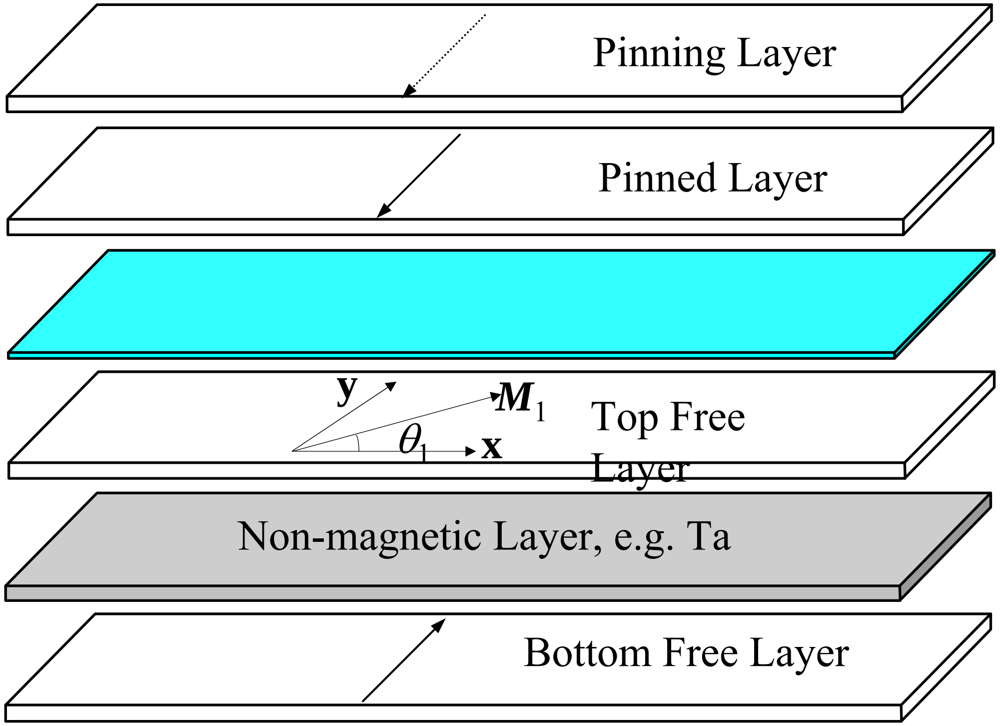
Outputs

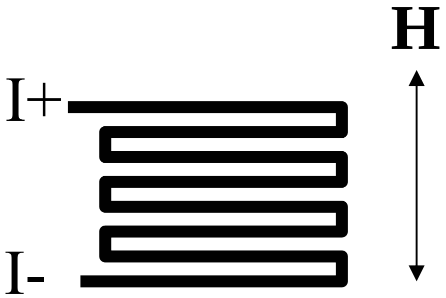

Sine and Cosine Output from AAV Sensors
Voltage Output (5V Supply)
2.58
2.56
2.54
2.52
2.5
2.48
2.46
2.44
2.42
0
90
180
270
360
Degrees of Rotation
Sine
Cosine

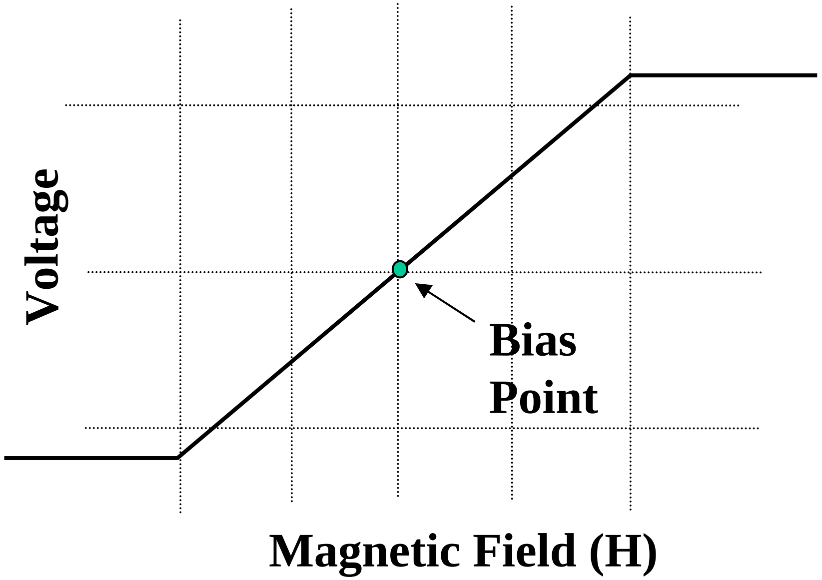
Linear Material Isolators

- **Original Product Line**
  - **Digital Spin Valve (Square Loop)**
  - **Retained Last Data State**
  - **Sometimes Not Desirable**
- **Use Linear Sensor**
  - **“Fail Safe” Off Position**
  - **Analog-Analog Isolator Possible**

"Z-Layer" Magnetoresistor

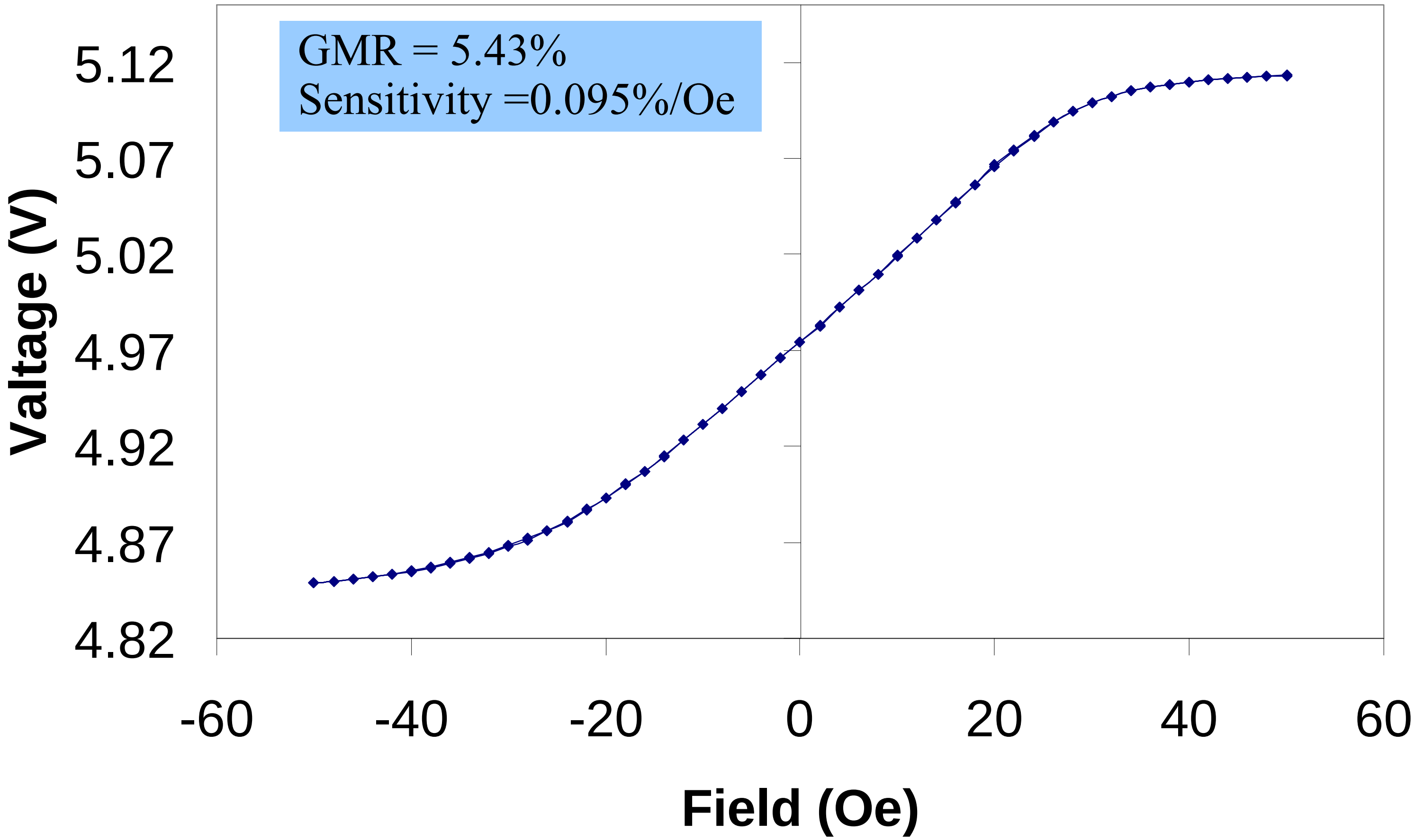




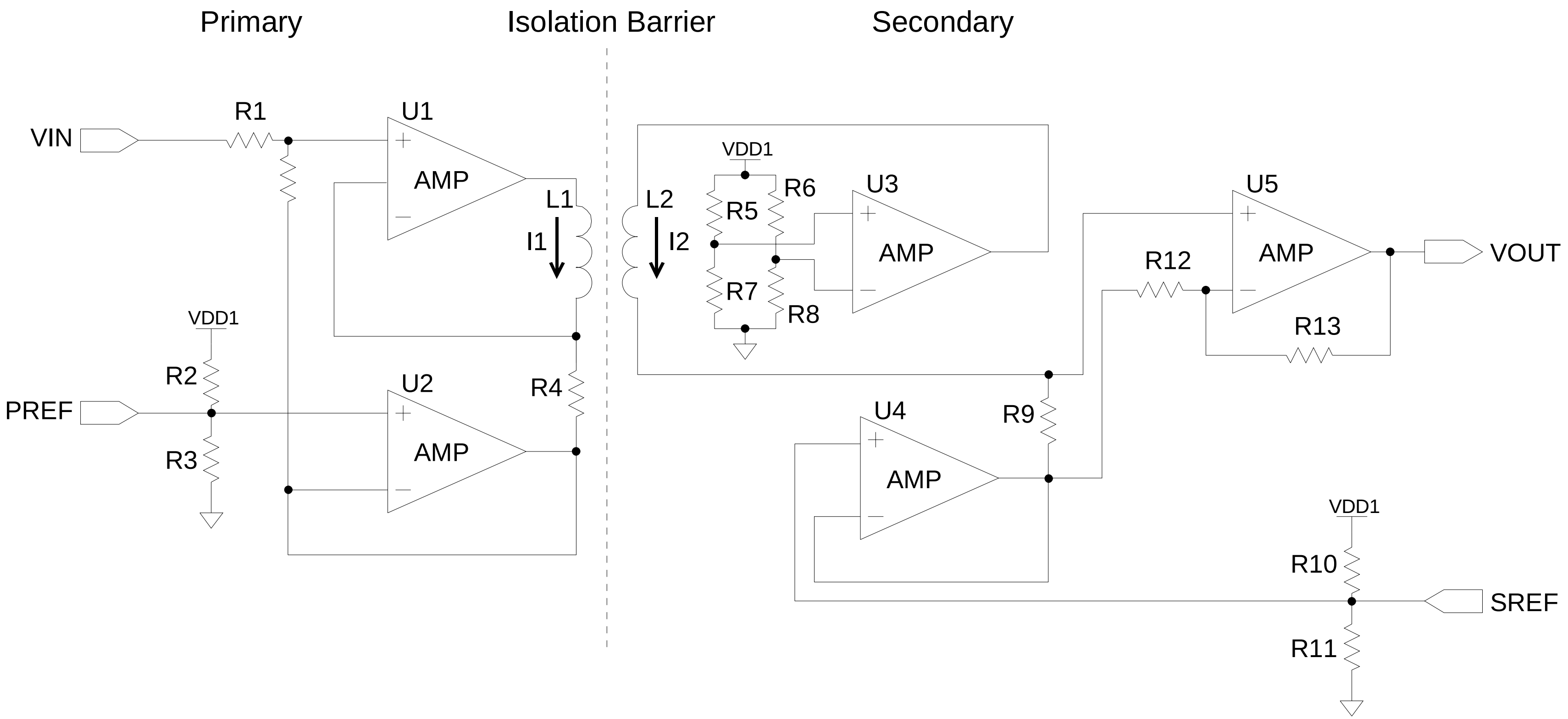


GMR Transfer Curve of 4 μm Serpentine Resistor

The spin valve is with a configuration of Ta30Å-NiFeCo35Å-Ta40Å-NiFeCo42.5Å-CoFe12.5Å-Cu25Å-CoFe43.5Å-CrPtMn325Å.

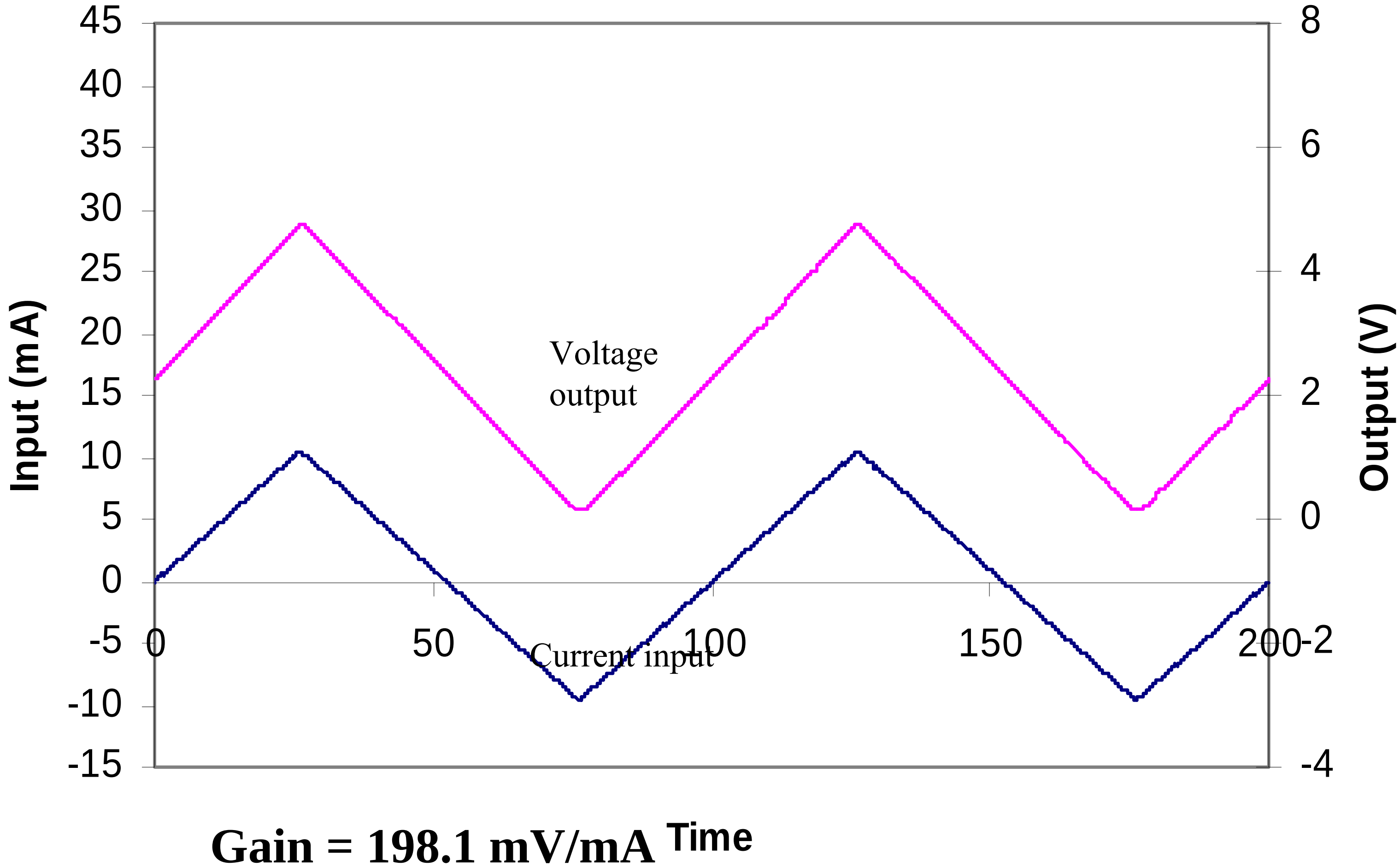


Circuit Schematic of Analog Isolator



On-chip feedback is used to improve linearity

Analog Isolator Performance



Gain = 198.1 mV/mA

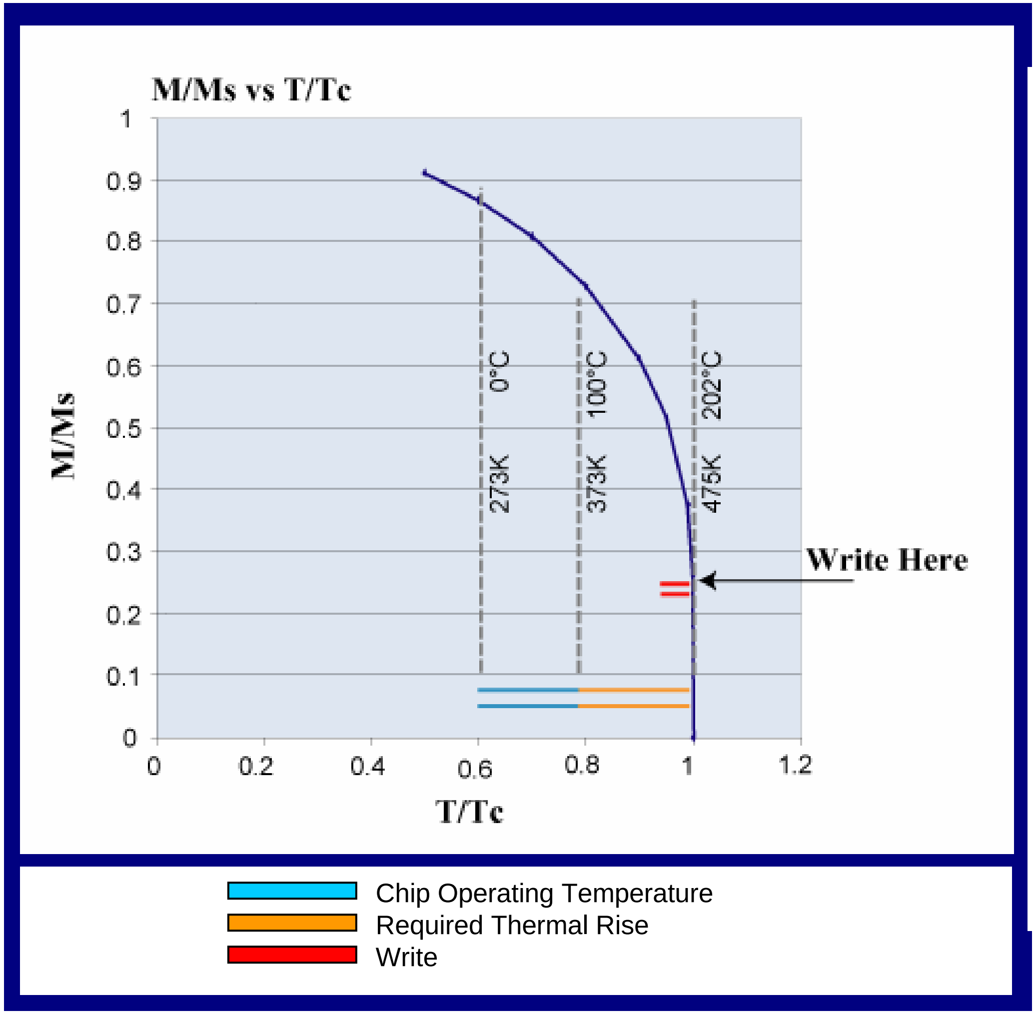
Linearity error < 0.3%

Thermal Limitations To MRAM Density

- Current Architecture
  - Shape Anisotropy - Storage Mechanism
  - 2D Array - Write Selection
  - Half-Selected Cells Least Stable, Dominate Failures
- High Areal Density Requires High Storage Energy*
  - Failure Rate Depends On $(1/\tau)e^{-Es/kT}$, τ switching time
  - Es ~ (1/8) (Volume)(Hk)(M) For Half-Selected Cells
  - Implies Thicker Films, Higher Shape Anisotropy
- Higher Currents, Temperature Rises
- 0.1 µm Lithography Approximate Limit

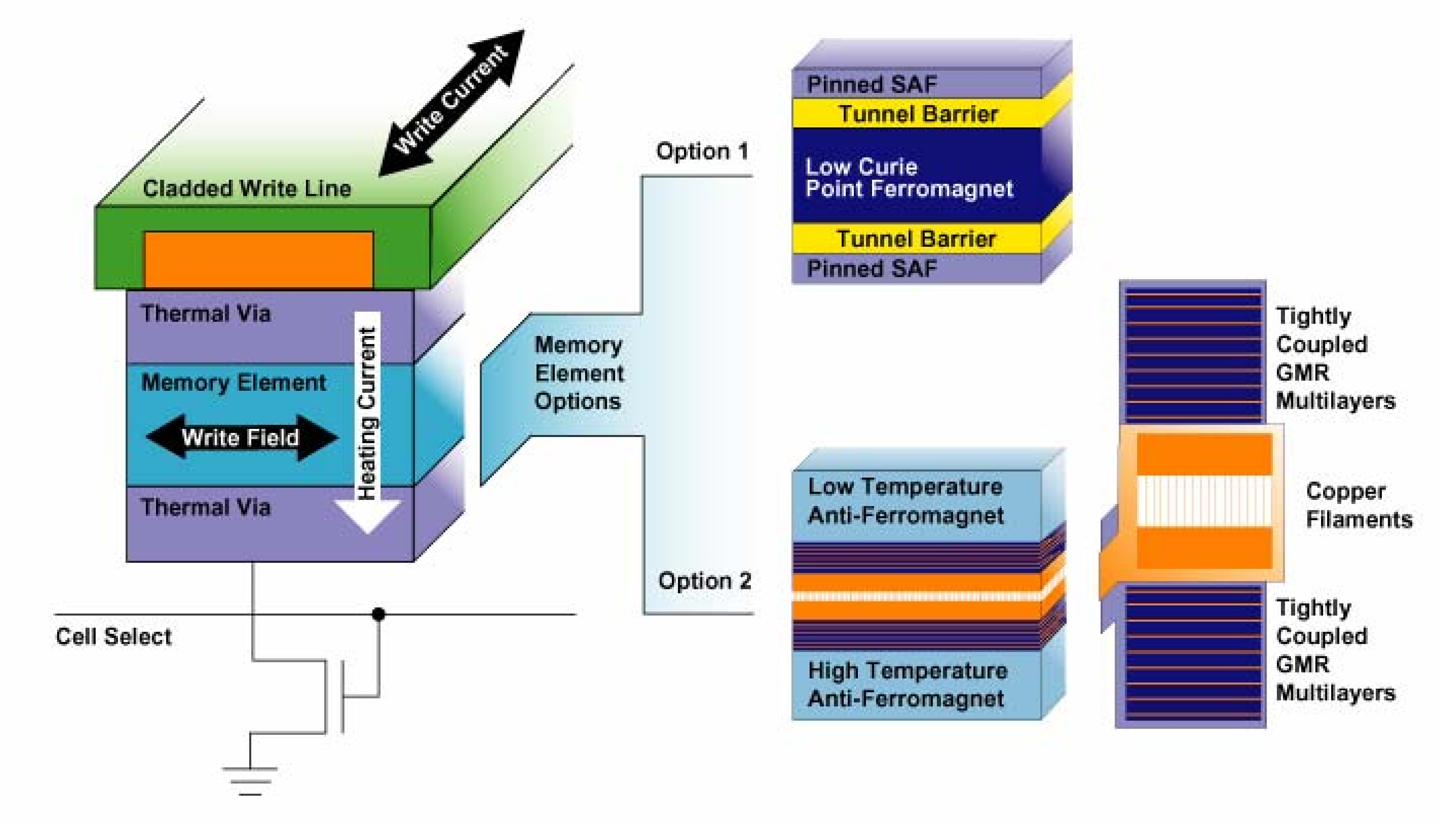
* **R. S. Beech, J. A. Anderson, A. V. Pohm, J. M. Daughton, "Curie Point Written Magnetoresistive Memory", JAP 87 #9, pp 6403-05, May 2000.**

Magneto-Thermal MRAM

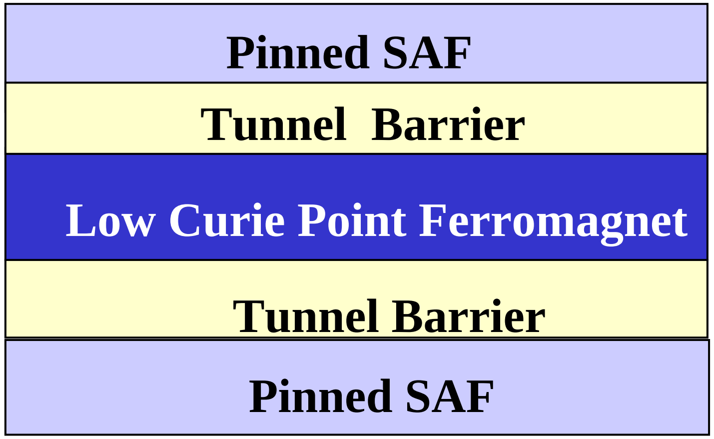


- Heat Magnetic Material Near Or Above Ordering Temperature
- Cool In Presence of Magnetic Field
- Result: Better Stability/Lower Currents

Two M-T Concepts

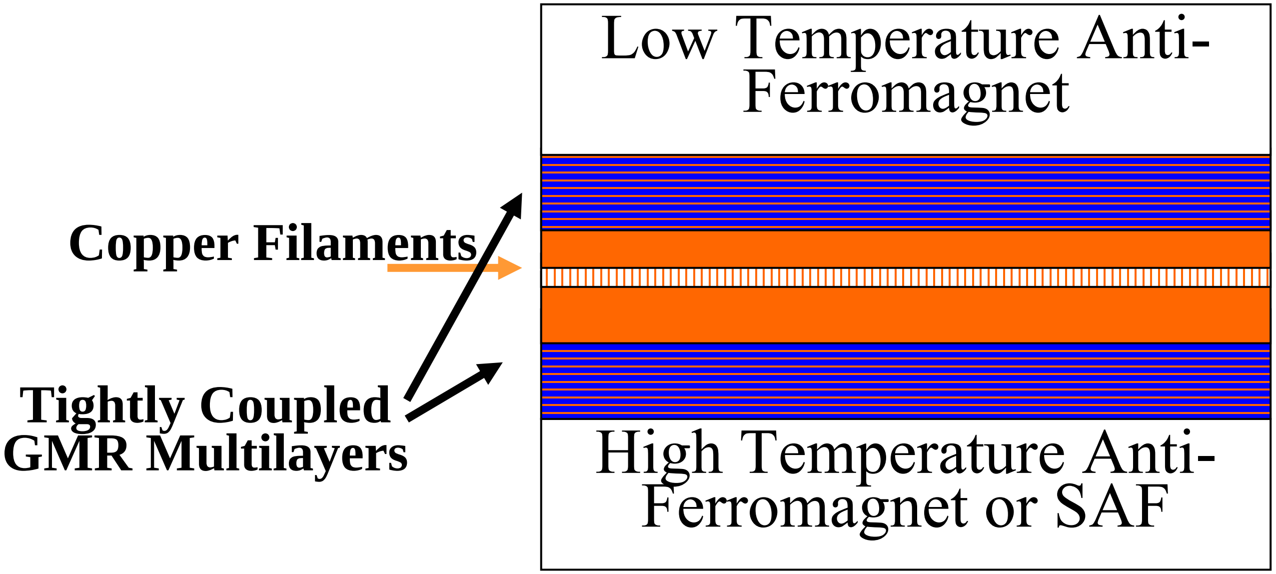


Curie Point/Tunnel Junction



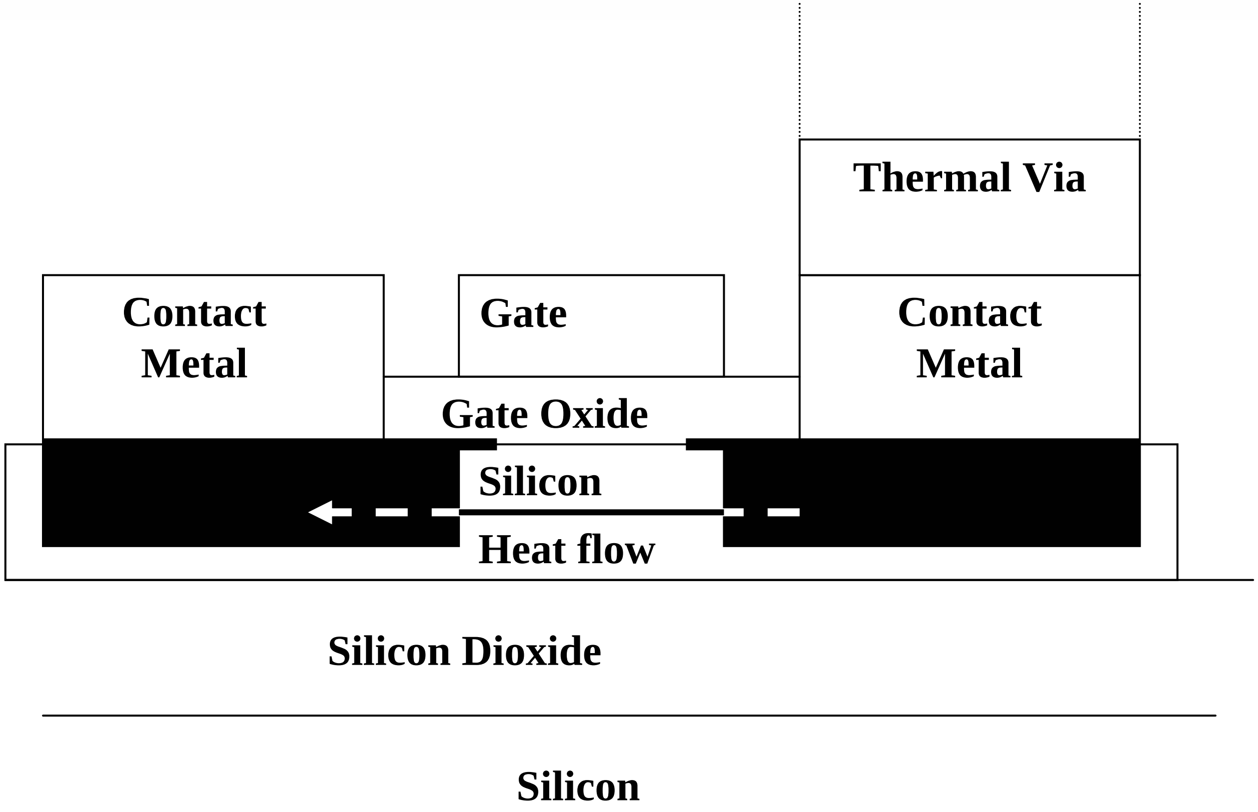
- Max Current 100 µA Minimum Xistor
- Maintain 50 ns Memory Cycle
- Two Junctions - Voltage Limited
- Low RAP Required (~10 Ω-µm^2)
- Tunnel Junction Reliability Risk

Nèel Point/Vertical Spin Valve



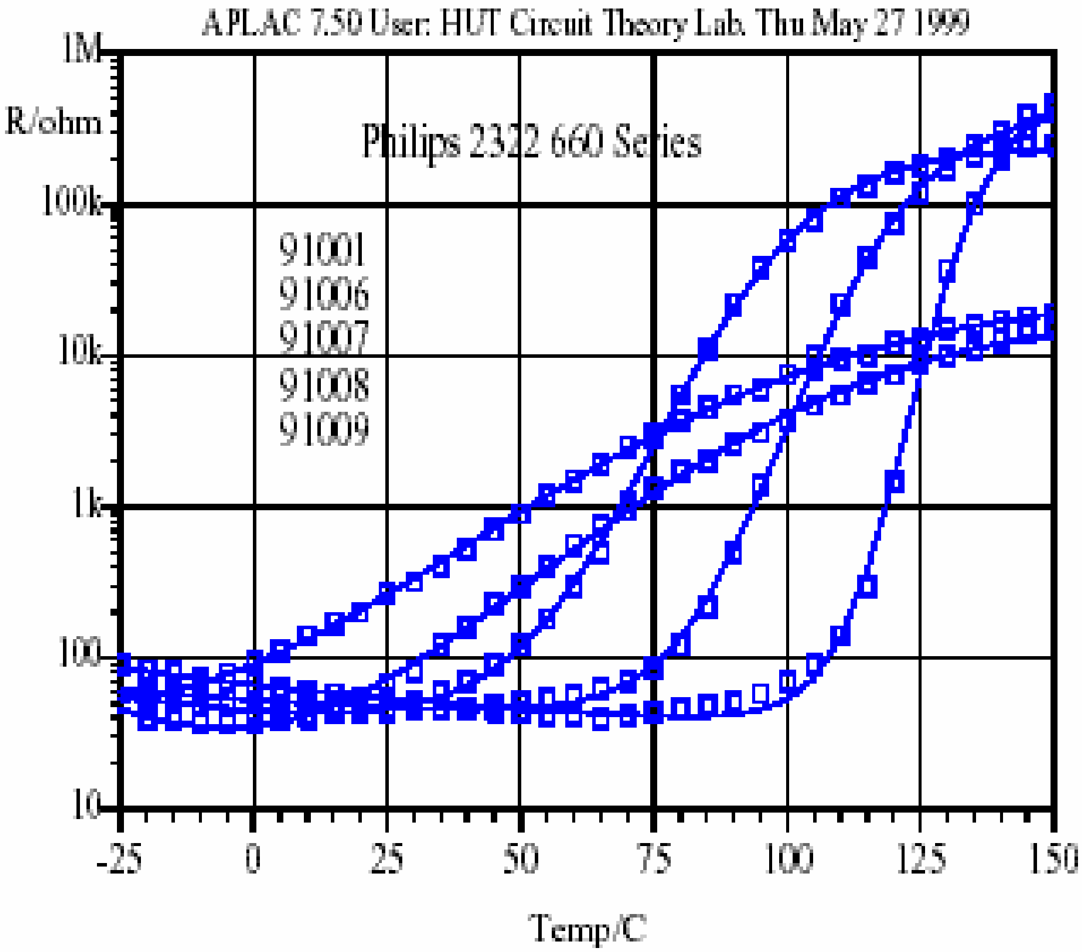
- Same Memory Requirements
- Copper Filaments - X1000 Higher Resistance
- Some Head Company Success (>X10)
- AF Material - Pinning Risk

New Idea - SOI Assisted



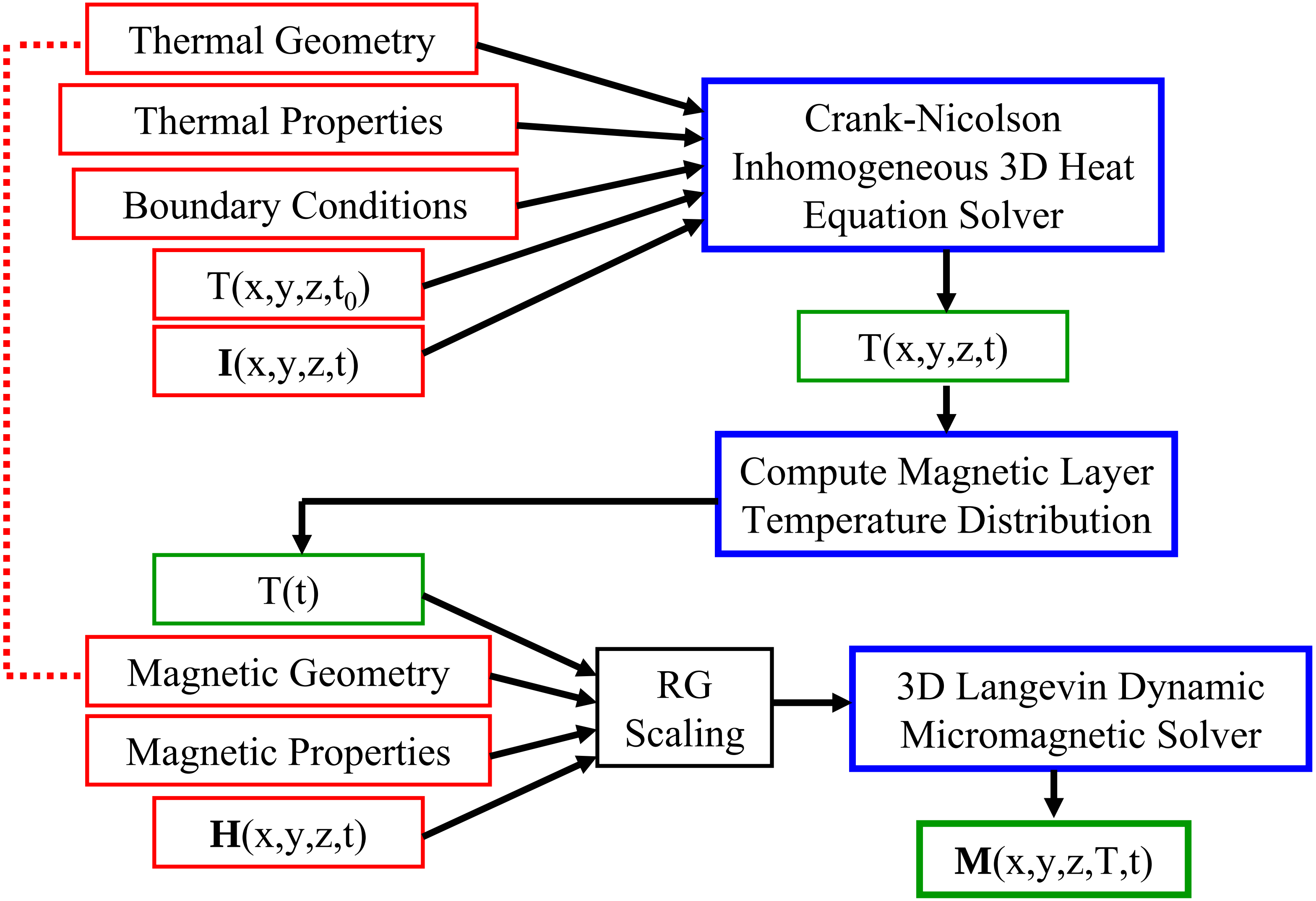
- Partial Heating From SOI Transistor/Diode
- 50 °C Thermal Rise Typical, 100 °C Common
- Reduces Heating Required in ME

New Idea - ThermistorAssisted



- Add Thermistor Next To ME
- Low R With Low Current
- High R With Higher Current

Simulation Overview - Jim Deak



Thermal Geometry

Thermal Properties

Boundary Conditions

$T(x,y,z,t_0)$

$\mathbf{I}(x,y,z,t)$

Crank-Nicolson Inhomogeneous 3D Heat Equation Solver

$T(x,y,z,t)$

Compute Magnetic Layer Temperature Distribution

$T(t)$

Magnetic Geometry

Magnetic Properties

$\mathbf{H}(x,y,z,t)$

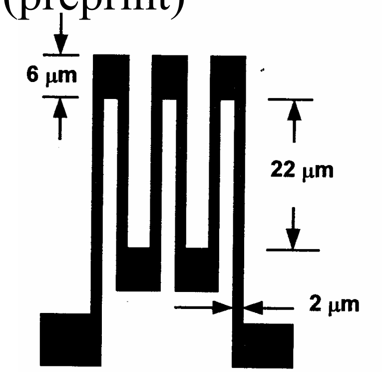
RG Scaling

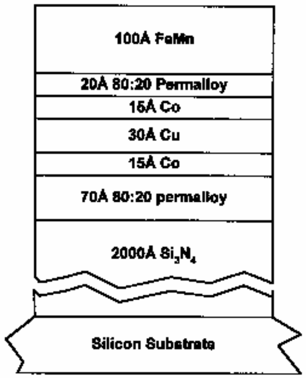
3D Langevin Dynamic Micromagnetic Solver

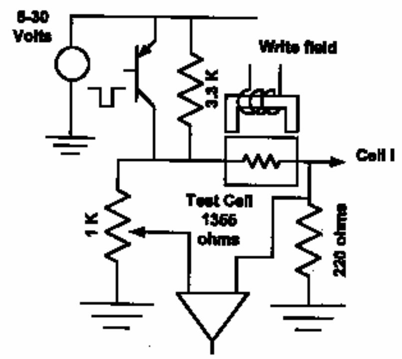
$\mathbf{M}(x,y,z,T,t)$

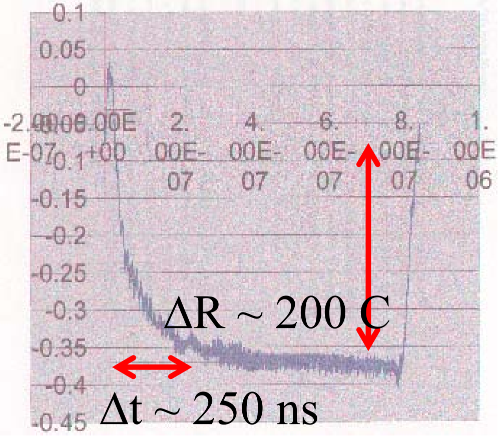
Thermal Code Qualification

Data from "*Durability of thermally written spin-valve memory cells*", A. V. Pohm, J. M. Daughton, R. S. Beech, and J. M. Anderson, (preprint)

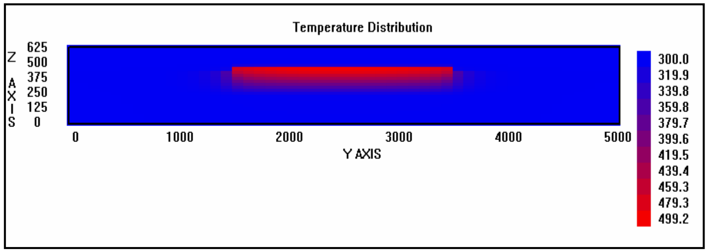




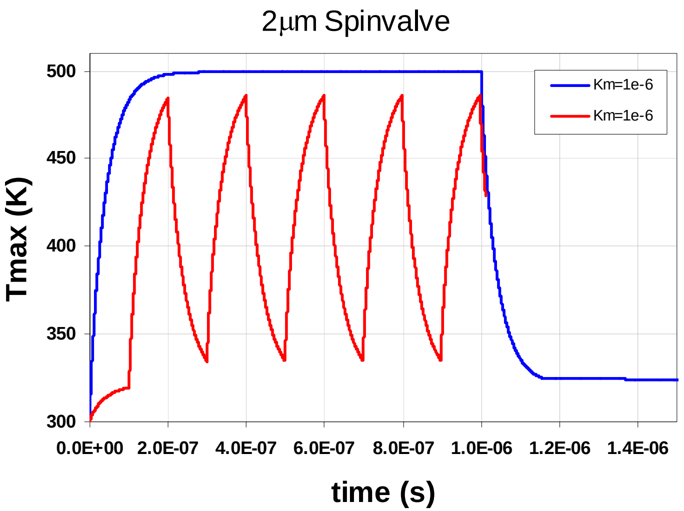




Simulate cross-section of spin-valve in paper using measured parameters

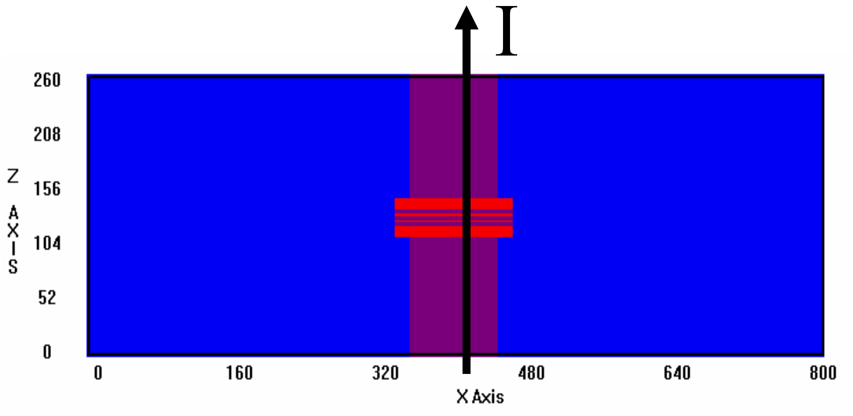


Result agrees with measurement



This is a large test structure, timescale not indicative of MT-MRAM device

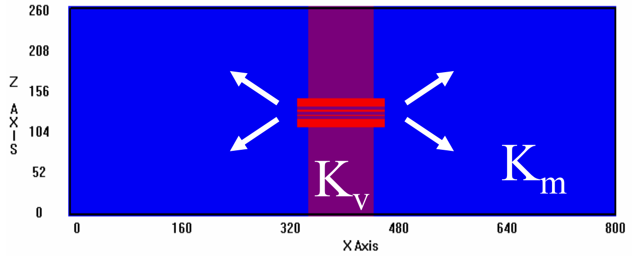
CPP Heating Mode



- Restrictions
  - <0.1 mA → cell size
  - <200 mV/MTJ → junction reliability

- Adding more resistors the stack increases heating efficiency and decreases stress on barrier
  - Reduces effective TMR
  - One Solution - Nonlinear PTC resistors - (thermistors)

Encapsulating Material Heat Leak

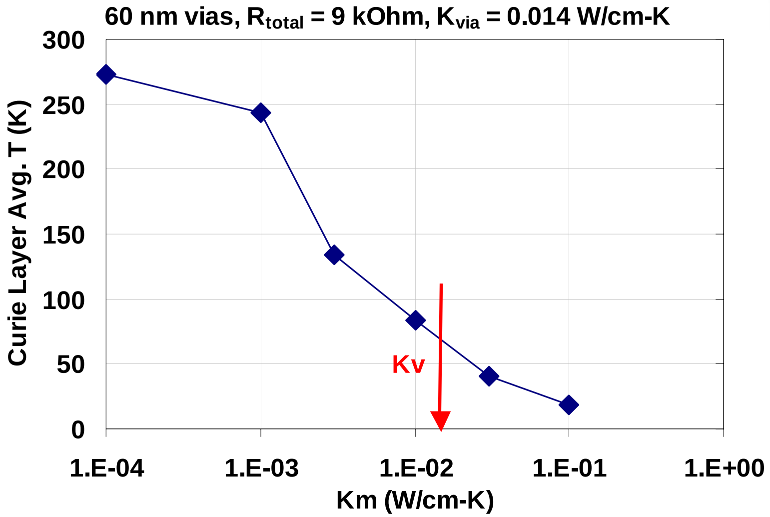


- Heat diffuses into the encapsulating material
→ Lowers heating efficiency

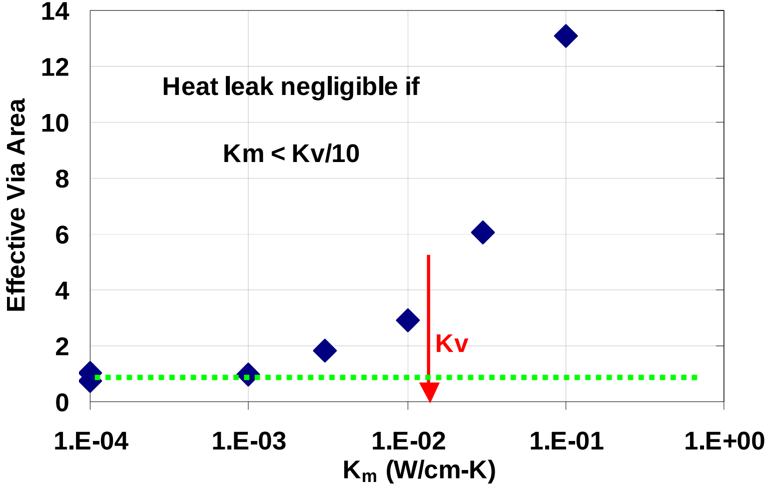
- Looks as if the thermal vias have a larger effective area

$$A_{eff} = \left(\frac{2K_v \Delta T}{PL}\right)\frac{1}{A_{via}}$$

60 nm vias, R_{total} = 9 kOhm, K_{via} = 0.014 W/cm-K



60 nm vias, R_{total} = 9 kOhm, K_{via} = 0.014 W/cm-K



Heat leak negligible if

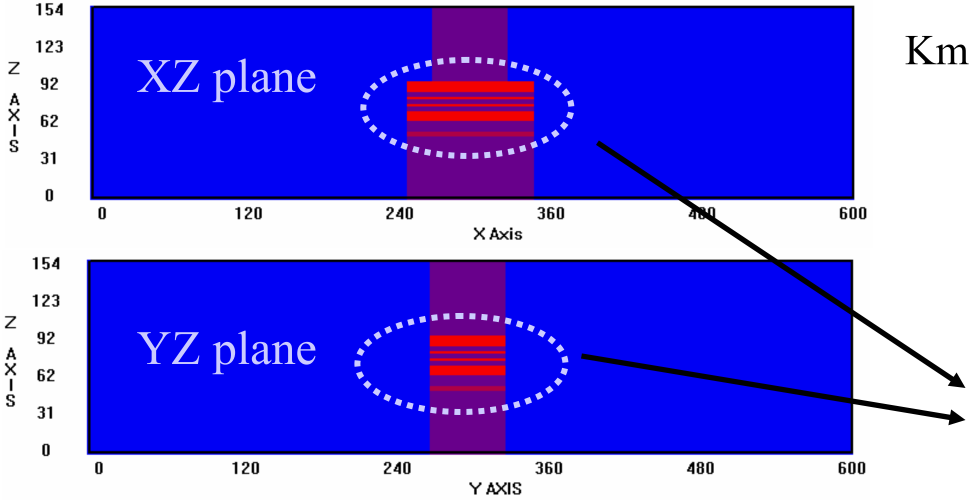
Km < Kv/10

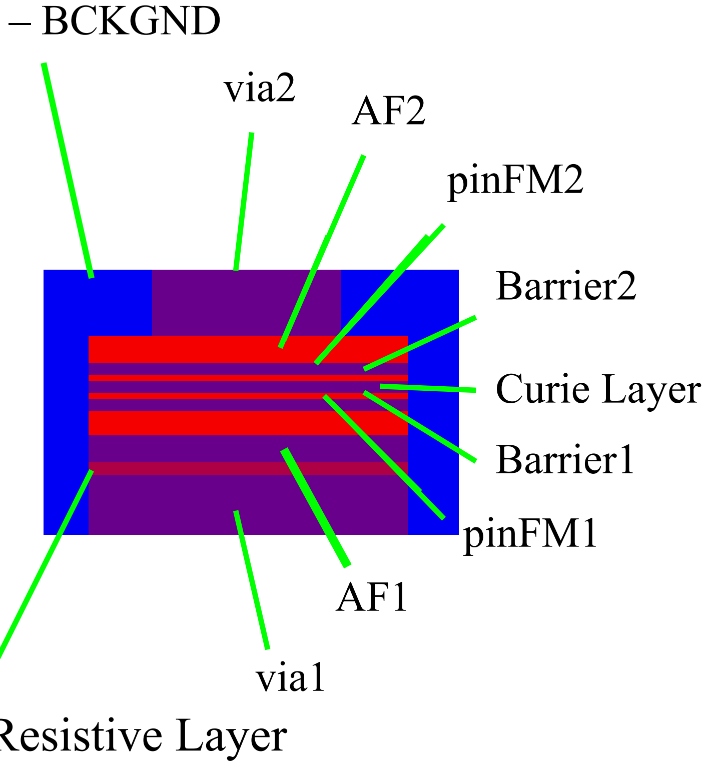
Best if K_m<K_v/10 → Use Organic insulating materials – polyamide? to encapsulate the bit and thermal vias

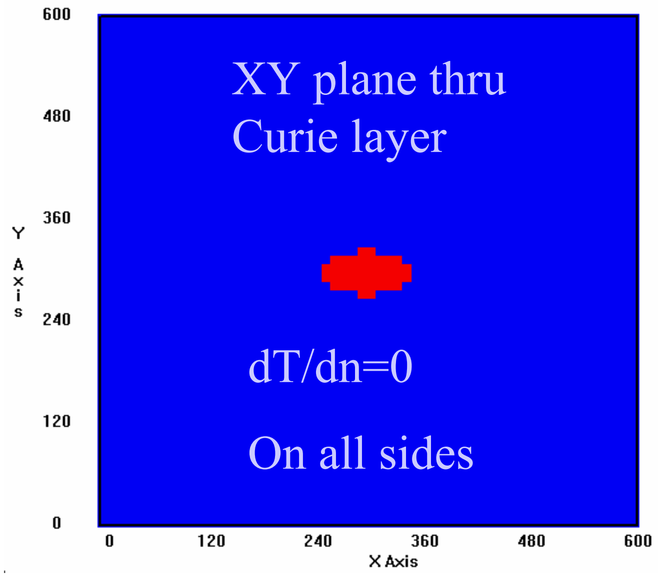
Curie Write Thermal Simulation Geometry

T=300 K top/bot

100 nm x 50 nm bit







Low I = Low T = READ

Large I = High T = WRITE

BaTiO as a PTCR Heater

- Barium titanate compounds show positive temperature coefficient resistivity (PTCR)

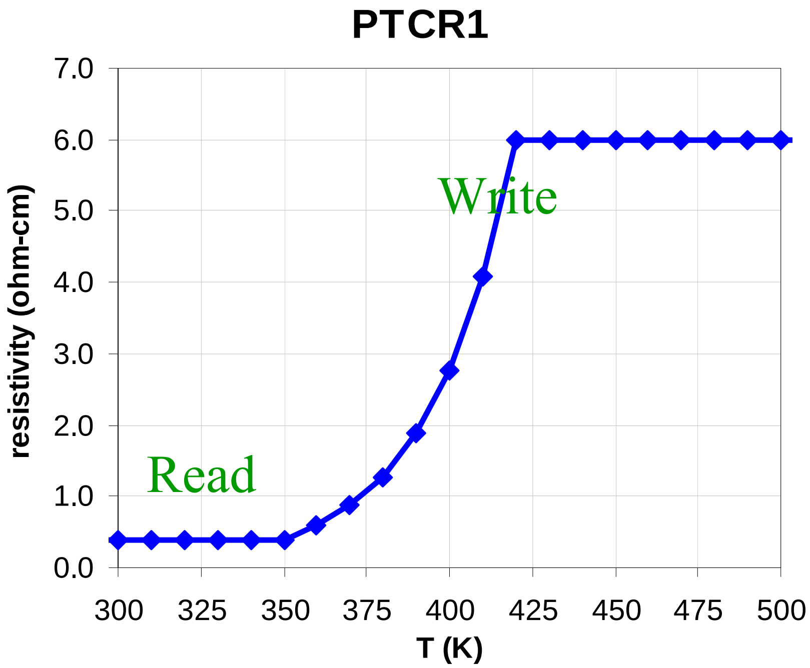
- Resistivity can very by order of magnitude over < 100 K range

- PTCR Associated with the ferroelectric Curie point of the material

- FE T_c depends on composition and film thickness – Transition suppressed below 2.5 nm

- Will a nanoscale thermistor work??

Curie Point MRAM Materials

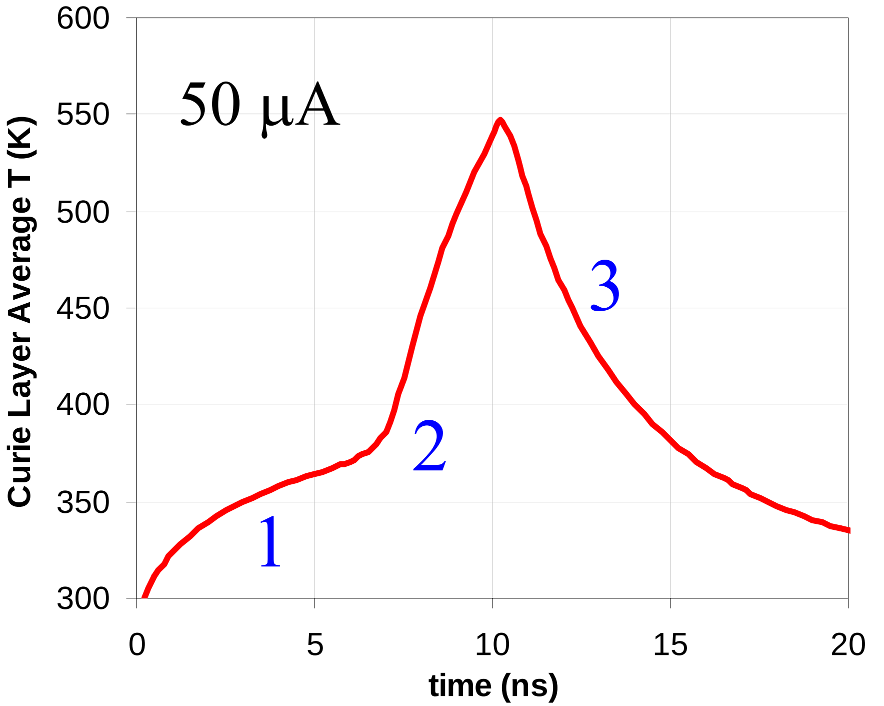


- PTC Resistive Layer ~ Doped BaTiO

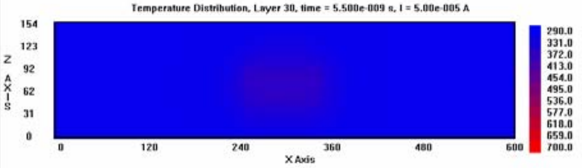
  T_c = 350 K depends on doping and layer thickness

- BCKGND K_m = 0.003 W/cm-K (organic insulating material)

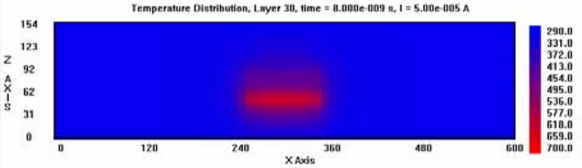
Joule Heating Using PTC Resistor



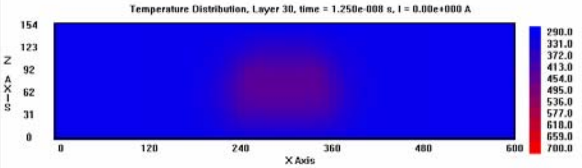
1. MTJs dominate below FE T_c



2. PTCR Above FE T_c, dominates



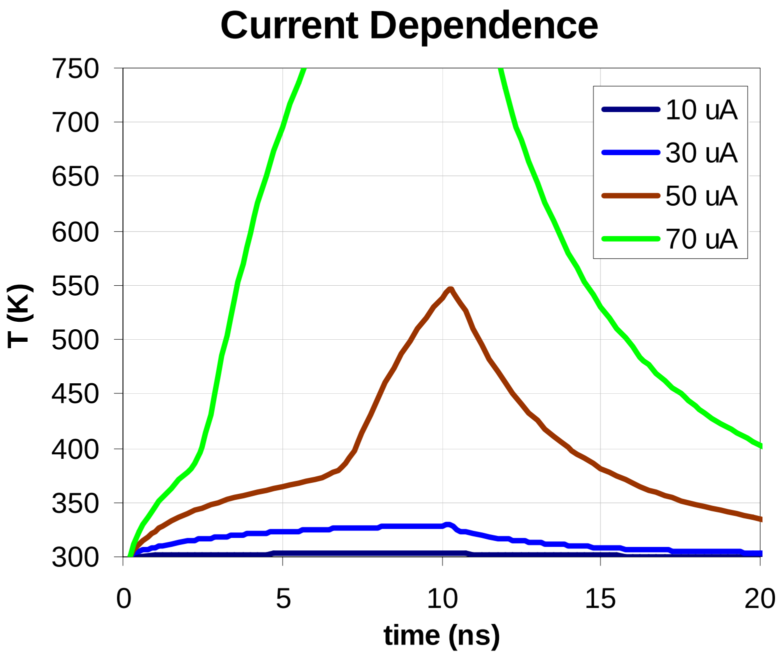
3. I=0, T drops



Heating simulated using temperature dependent resistance of PTC layer

Cross over at 375 K

Curie Point MRAM Thermal Results (100 nm x 50 nm bit)



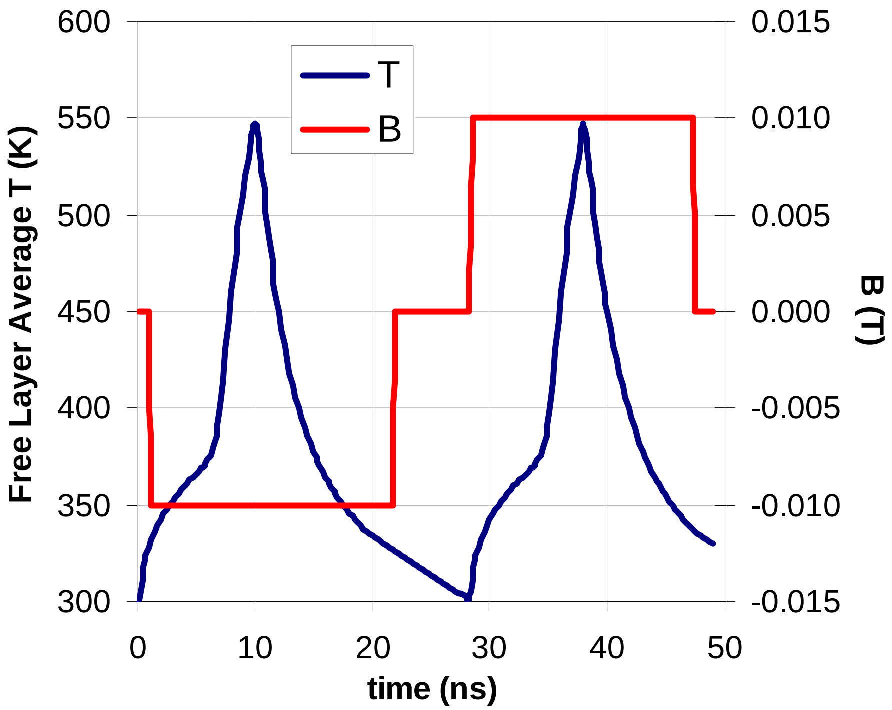
- Simulated heating as a function of current pulse magnitude
- Heating current applied for 10 ns
- MTJ RAP ~ 15 Ωμm^2
- **Max Current for 200 mV ~ 52 μA**
- Curie Layer T_c ~ 500 K

Possible to achieve 200 C temperature differential at 50 μA without exceeding 200 mV across the junction!

Read current ~ 30 μA without significant heating

TMR during read not affected by PTCR

Curie Pt Write Sequence -100 nm x 50 nm



Thermal response calculated for

- –60 nm vias
- –PTCR Layer
- –Two MTJ barriers
- –50 μA heat current

- •Start with bit magnetized in positive X direction
- •Apply heat current
- •Turn on the field
- •Turn off heat current
- •Turn off the field when bit is sufficiently cool

Curie Point Writing Simulation

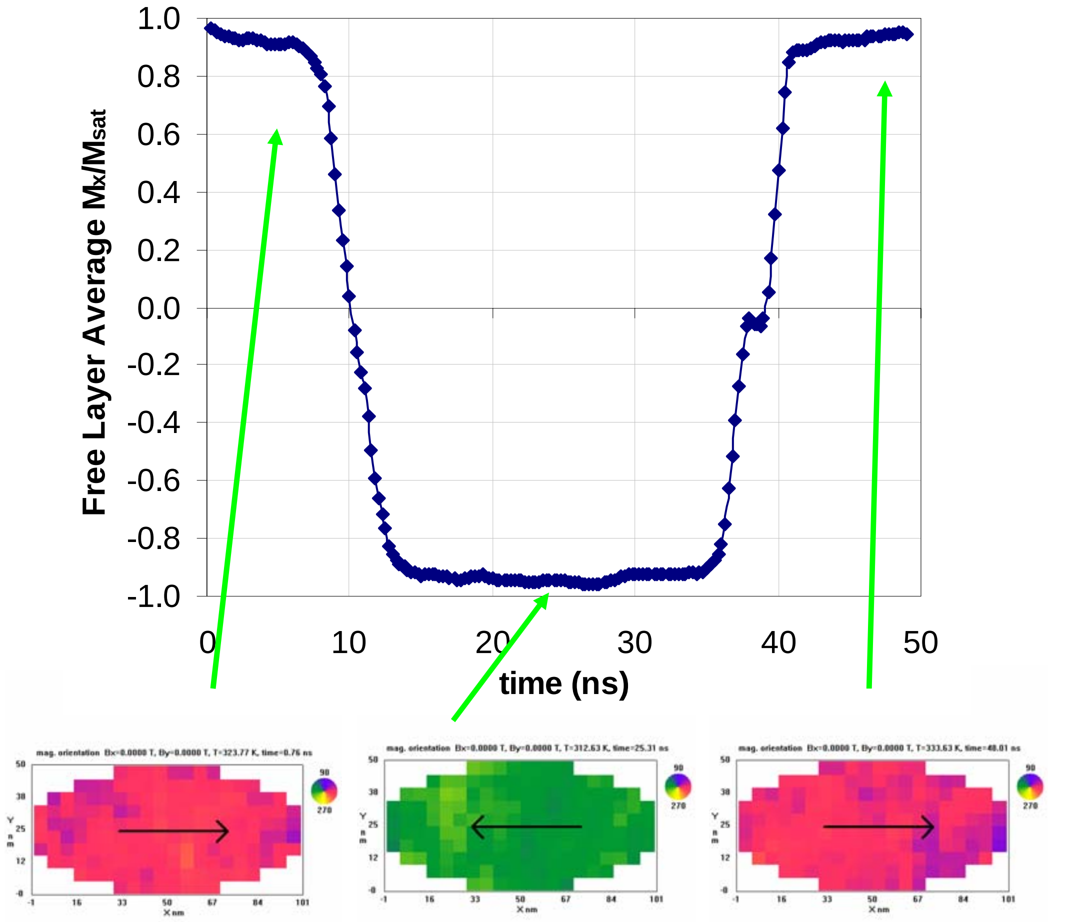
100 nm x 50 nm dot

H_{write} = 100 Oe

I_{heat} = 50 μA

Ferromagnet

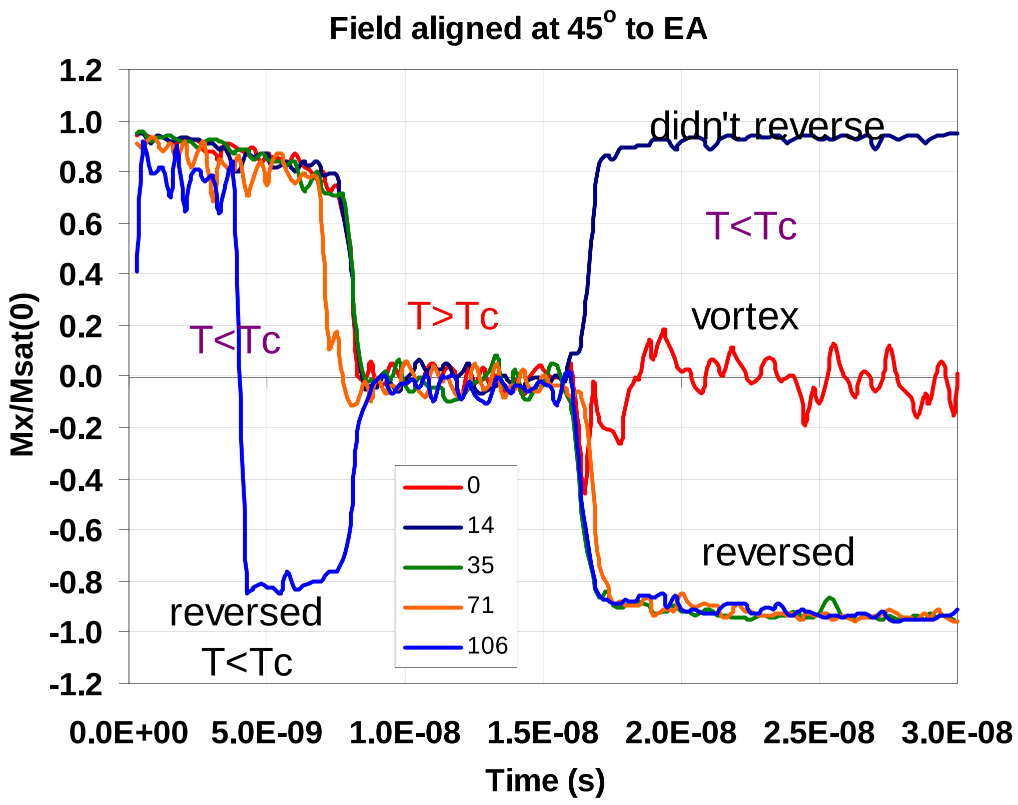
- 5 nm thick (thicker yields vortices)
- H_k = 2.5 Oe
- T_c = 500 K
- M_{sat} = 800 emu/cc



Snapshots of zero field states

Curie Point Writing, Simulation

Generalized Behavior



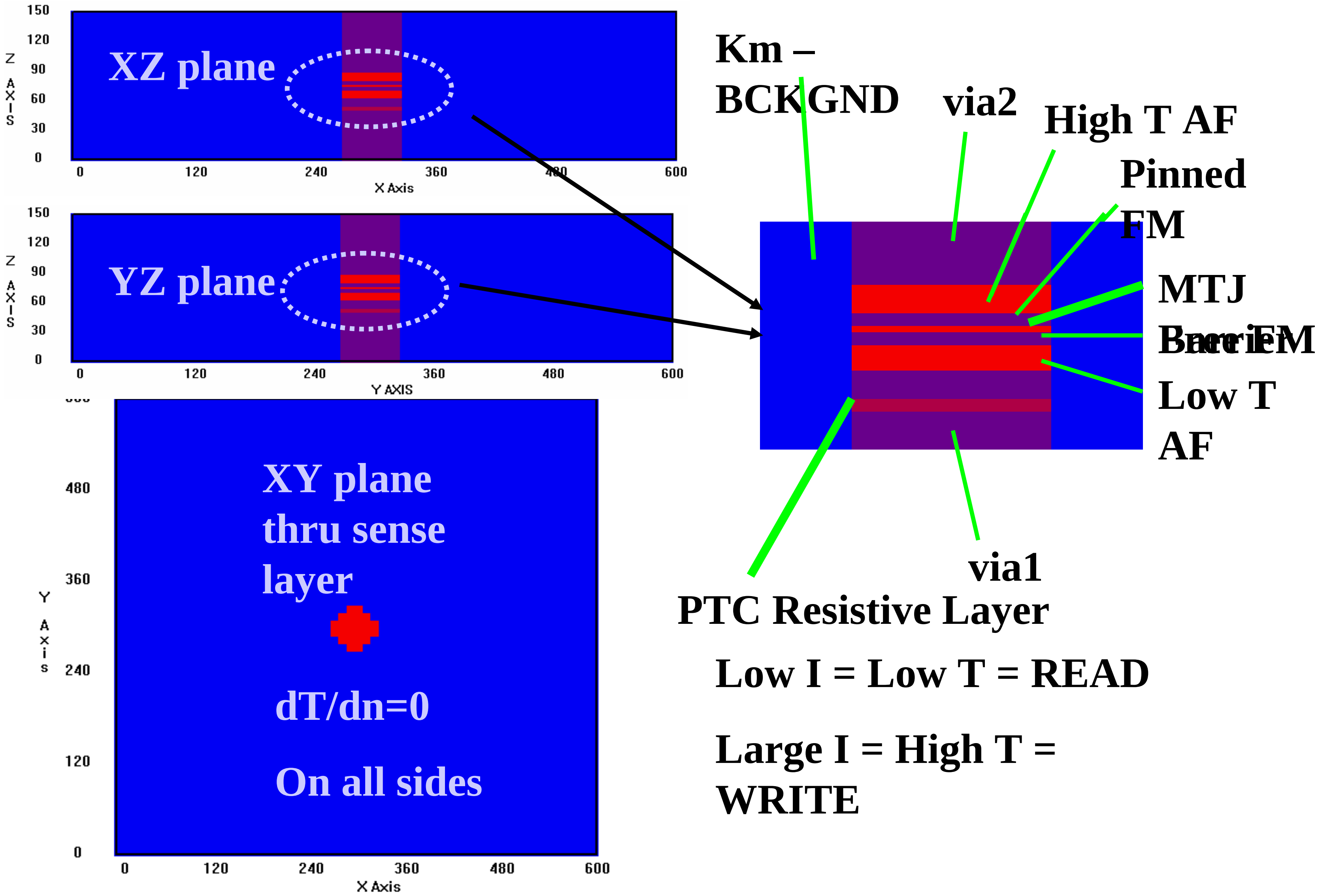
Three different behaviors predicted, dependent on switching field strength

- ***Low H***, bit may freeze into a vortex
- ***Intermediate H***, bit freezes into reversed state on cooling
- ***High H***, bit reverses below T_c

Neel Write Thermal Simulation Geometry

T=300 K

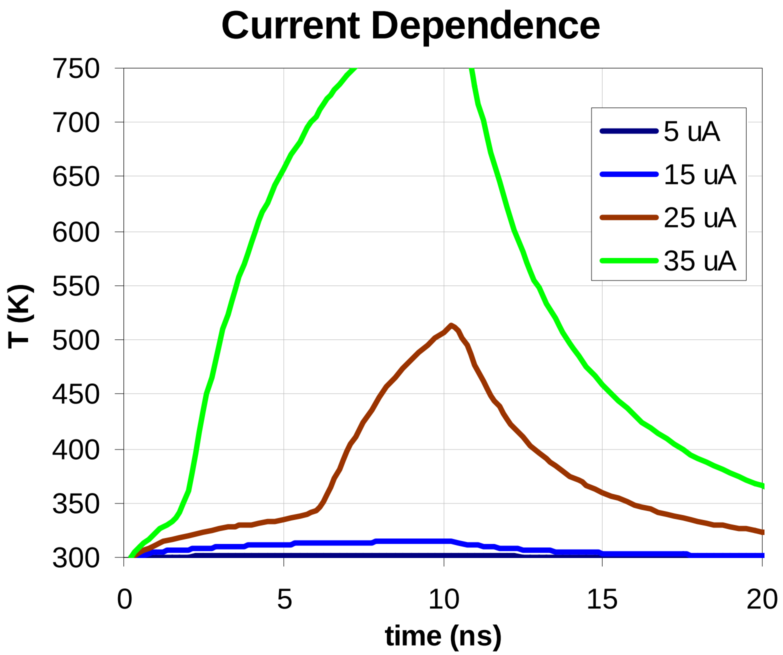
50 nm x 50 nm bit



Low I = Low T = READ

Large I = High T = WRITE

Neel Thermal Results - 50 nm x 50 nm bit



- Simulated heating as a function of current pulse magnitude
- Heating current applied for 10 ns
- MTJ RAP ~ 15 Ωμm^2
- **Max Current for 200 mV ~ 26 μA**
- Low T_N AF ~ 470 K

Possible to achieve 200 C temperature differential at 25 μA without exceeding 200 mV across the junction!

Read current ~ 15 μA without significant heating

Effective TMR reduced by 60% due to PTCR (double MTJ would be preferred to heat PTCR above FE T_c)

Neel Point Writing Simulation

50 nm dot

H_{write} = 100 Oe

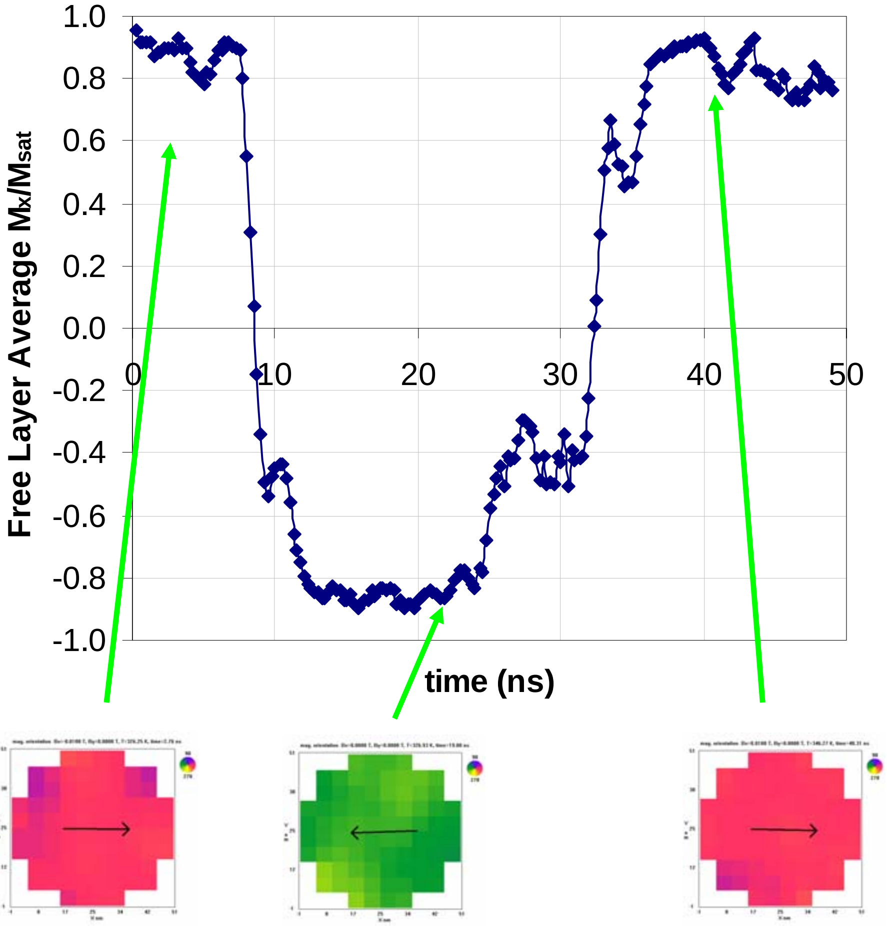
I_{heat} = 25 μA

Ferromagnet

- 3 nm thick (thicker yields vortices)
- H_k = 2.5 Oe

Low T_N Antiferromagnet

- T_b = 470 K
- H_{pin} = 200 Oe



Snapshots of zero field states

M-T Compared To Other Approaches

- Primarily Material Risks
  - Wear Out - Thermal Cycling
  - Junction Reliability (MTJs)
  - RAP Levels (SV Multilayers)
  - Nanoscale Thermistors
- Lower Currents Than Other Modes
- Saves A Contact Per Cell
- More Photographically Tolerant Than Stacked SAFs