Circuit Considerations for Spin-Switched MRAM Devices

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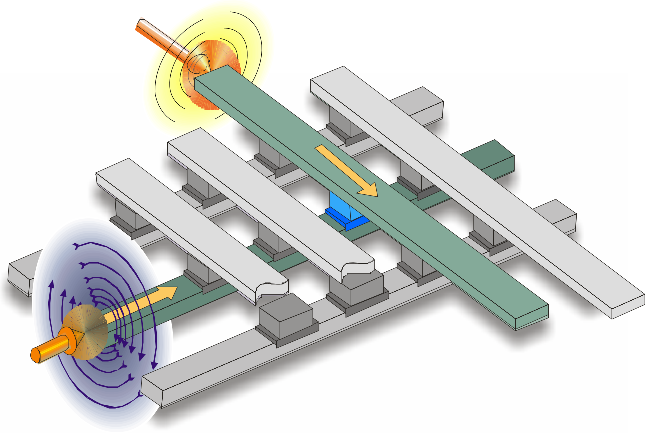
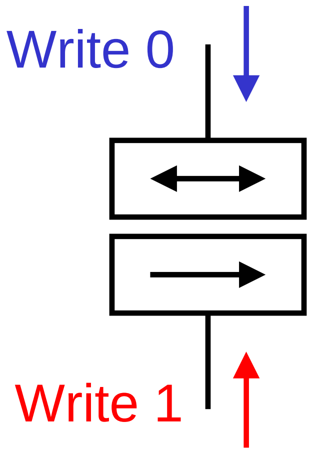
Introduction



- Conventional MRAM written by magnetic fields
  - Generated by currents passing across cell
  - Read / write mechanisms relatively distinct
- Spin-switched MRAM written by spin-transfer
  - Achieved by tunneling current through MTJ
  - Read / write coupled - both use tunneling current
  - Potential advantages but new design challenges
- What array architecture & device characteristics are required?
  - To make spin-switched MRAM an attractive option



Current State of MRAM

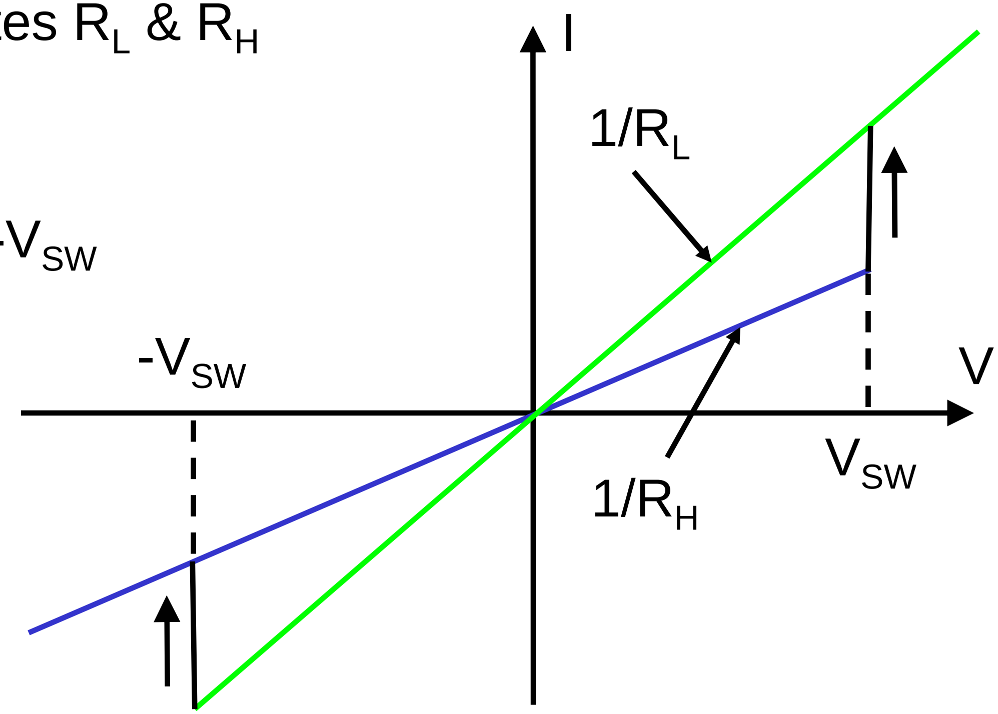
- Density - cell area ~ 1.5λm^2 in 0.18λm technology [1,2]
- Performance - read access/cycle, write cycle ~ 20-40ns
- Power
  - Data retention, standby - excellent
  - Read active - competitive with other memories
  - Write active - relatively high, dominated by write currents
- Process adder
  - ~ 3-5 masks & changes to 2 metal levels
- Device parameters
  - R_{MTJ} ~ 10KΩ, MR ~ 20-40% at V_{MTJ} ~ 250mV
  - Write currents ~ 1-10mA for ~ 5-10ns

Potential Advantages of Spin-Switching

- Lower active write current / power
  - Power dissipated in cell vs. along BL / WL
- Improved write margin
  - Ability to write selected cell without disturbing others
  - Eliminate BL / WL half select, adjacent BL / WL coupling effects
- Reduced process adder
  - ~ 1-2 masks with no changes to metal levels
- Improved density
  - Eliminate adjacent contact - can contact from below
  - Larger arrays - currently limited by BL / WL IR drops
- Scalability?
  - How do MTJ size & write current scale, incl. thermal SER effects?

Spin-Switched MTJ Current-Voltage Characteristic

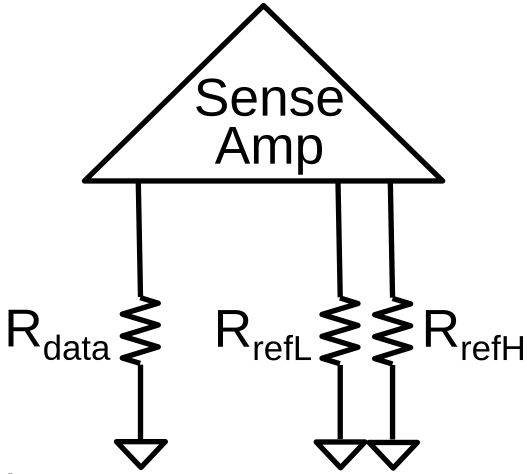
- Ideally
    - Two linear resistance states R_L & R_H
    - $R_H = R_L \times (1 + MR)$
    - Hysteretic switching at $+/-V_{SW}$
- In reality, probably
    - Non-linear
    - Non-constant MR
    - Non-symmetric



- Some of these non-idealities may be good
- $V_{SW} > V_{RD}$ with margin to prevent read disturbs

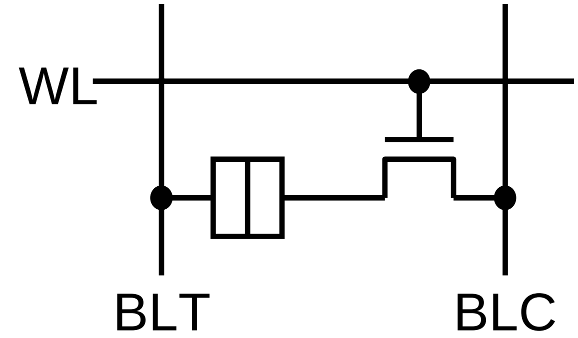
Sensing Considerations

- Assume data, reference sensed concurrently - simplest, fastest (<~50ns)
  - Apply V, measure I
  - Reference = average of L & H reference cells
  - Relative signal = I_{SIGNAL} / I_{REF} = MR / (MR + 2) ~ MR / 2
- Must consider local matching of MTJs & FETs
  - ρ of $\Delta R_{MTJ} / R_{MTJ}$ ~ 1%
  - ρ of $\Delta I_{DS} / I_{DS}$ ~ 1%
  - ρ of ΔV_T ~ 1mV

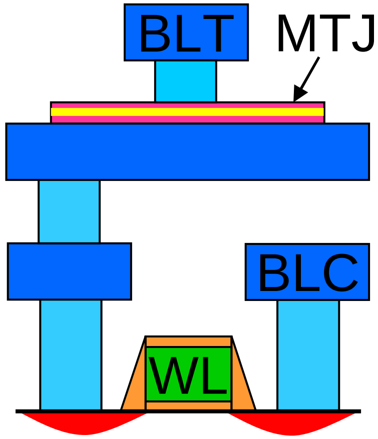


- Yieldable multi-Mb design requires
  - MR / 2 > ~ 4ρ of $\Delta R_{MTJ} / R_{MTJ}$ → MR > ~ 8%
  - MR / 2 > ~ 3ρ of $\Delta I_{DS} / I_{DS}$ → MR > ~ 6%
  - MR / 2 > ~ 3ρ of $\Delta V_T / V_{RD}$ → MR > ~ 6% if V_{RD} ~ 100mV
- MR > ~ 10%, V_{RD} > ~ 100mV plus margin

1T1MTJ Array Architecture



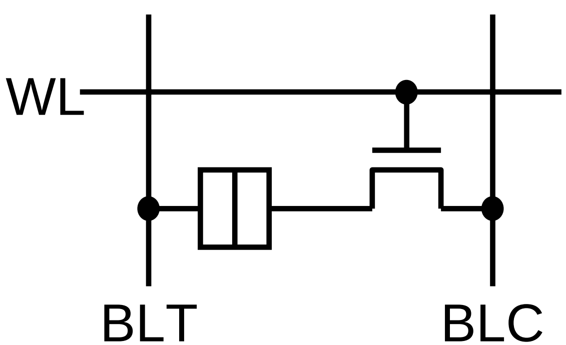
- Operation
  - Read: WL = V_{DD}, BLT/C = V_{RD} / GND
  - Write 1: WL = V_{DD}, BLT/C = V_{DD} / GND
  - Write 0: WL = V_{DD}, BLT/C = GND / V_{DD}
- Read
  - Similar to conventional MRAM
  - R_{MTJ} >> R_{FET} (~1KΩ) to avoid effective MR loss

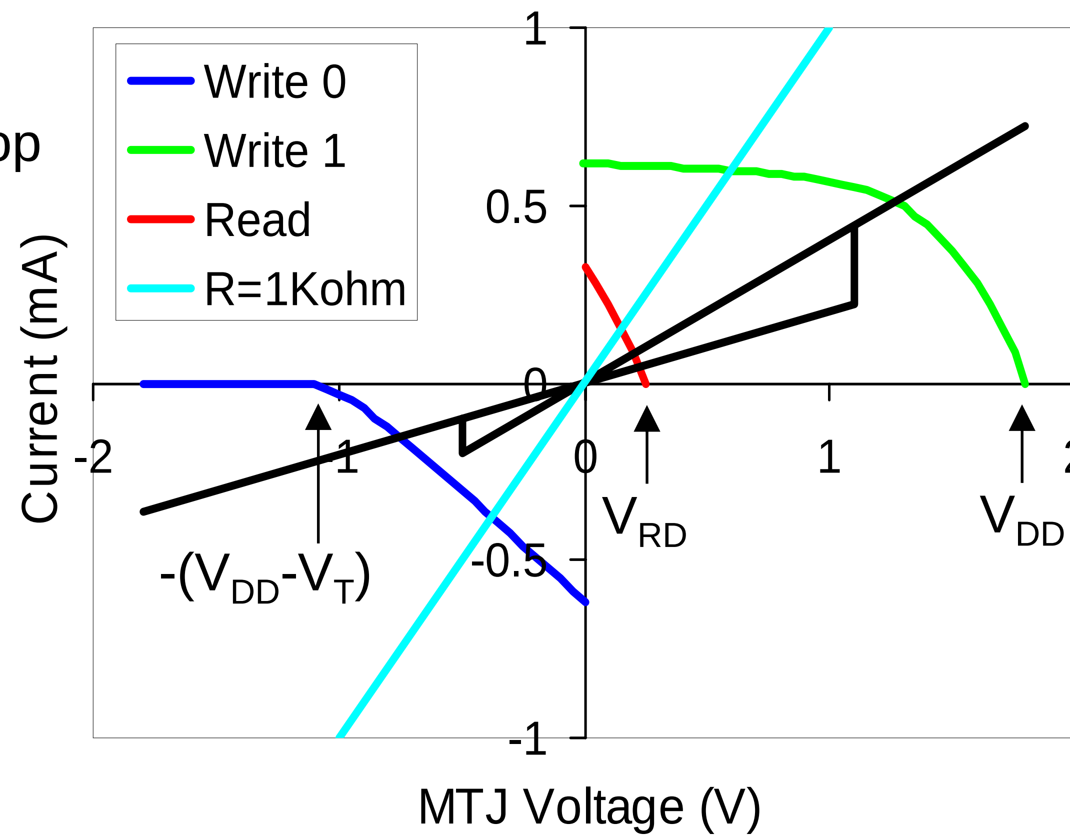


- Write
  - Unlike conventional MRAM, write current limited by cell FET
  - Particularly in Write 0 - FET turns off at $V_{MTJ} = V_{DD}-V_T$

1T1MTJ Array Architecture (continued)

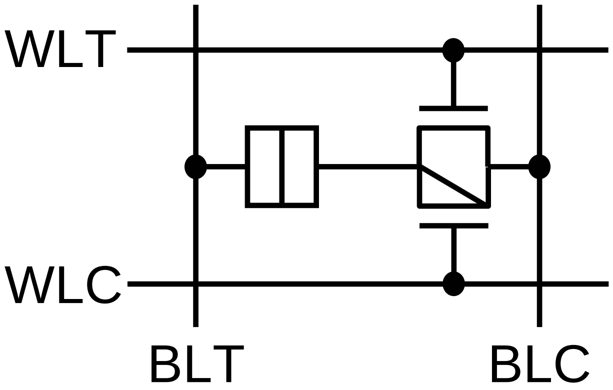
- FET load lines shown - W/L = 1.0λm/ 0.18λm, V_{DD} = 1.8V, V_{RD} = 0.25V
- MTJ hysteresis loop must fit inside write load lines with margin
- $V_{SW1} < V_{DD}$, $V_{SW0} < V_{DD} - V_T$, $I_{SW} <$ ~ 0.5mA
- Asymmetric IV may be good
    - Allows larger hysteresis loop
- Non-linear IV may be good
    - Allows larger R_{MTJ}, I_{SW}

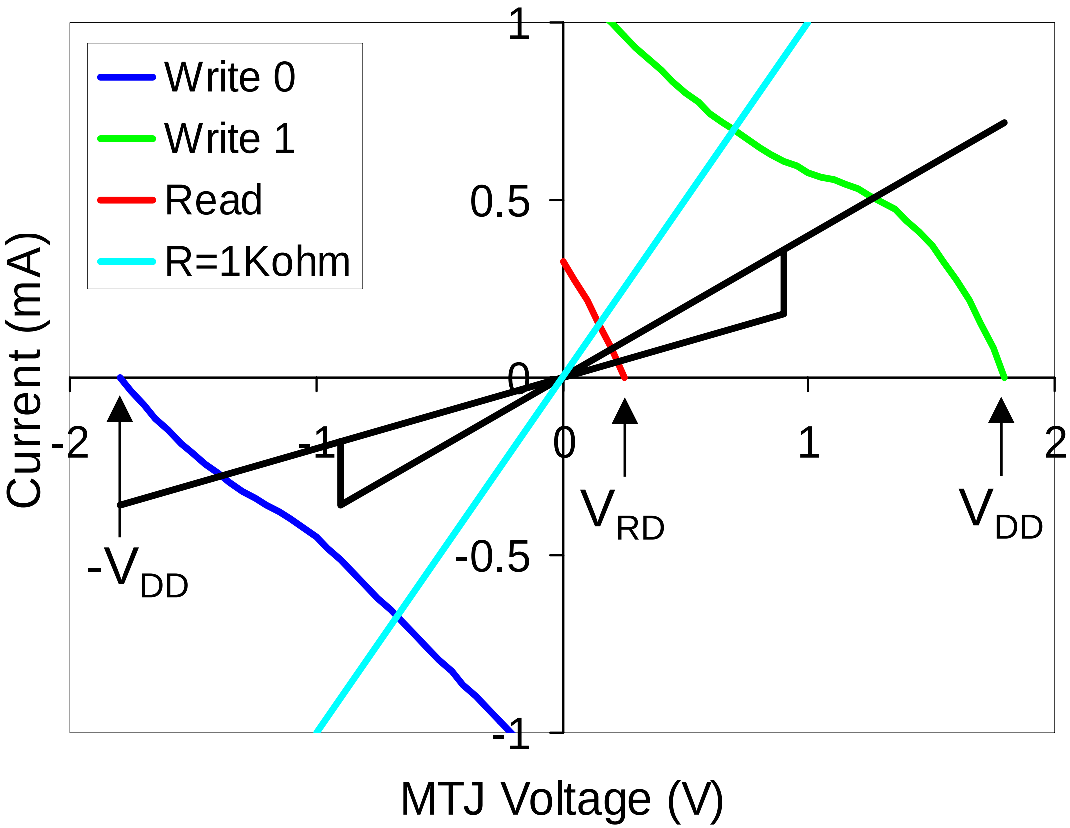




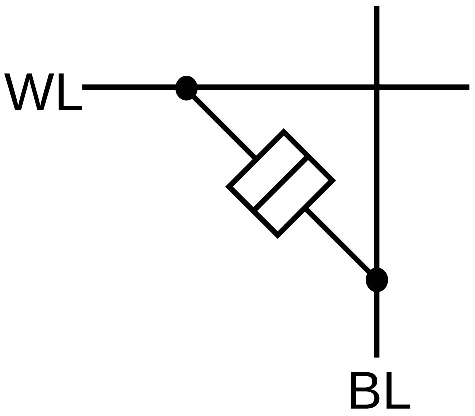
2T1MTJ Array Architecture

- Use CMOS transfer gate ($W_P/W_N = 2.0\lambda m/1.0\lambda m$)
- More symmetric switching at cost of density - still denser than SRAM
- $V_{SW} < V_{DD}$, $I_{SW} < \sim 0.5mA$
- Non-linear IV may be good
  - Allows larger R_{MTJ}, I_{SW}
- Attractive for learning vehicle?



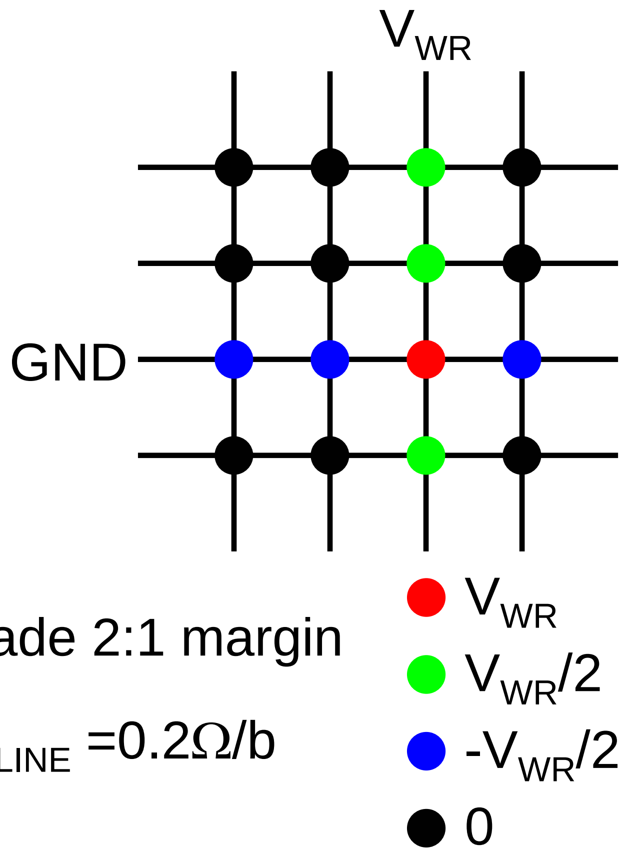


Cross-Point Array Architecture



- MTJ at each intersection of BL & WL
- The "Holy Grail" of memory array architectures
    - Dense - No FET to limit cell size
    - Stackable - Reduce cell size by 1 / # layers
    - Place circuits below array
- "Many have died seeking the Grail..."
    - Poor selection mechanisms for read / write

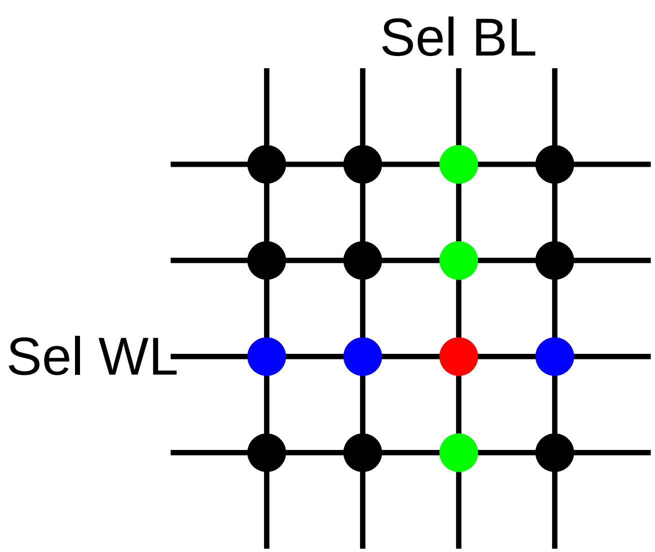
Cross-Point Write

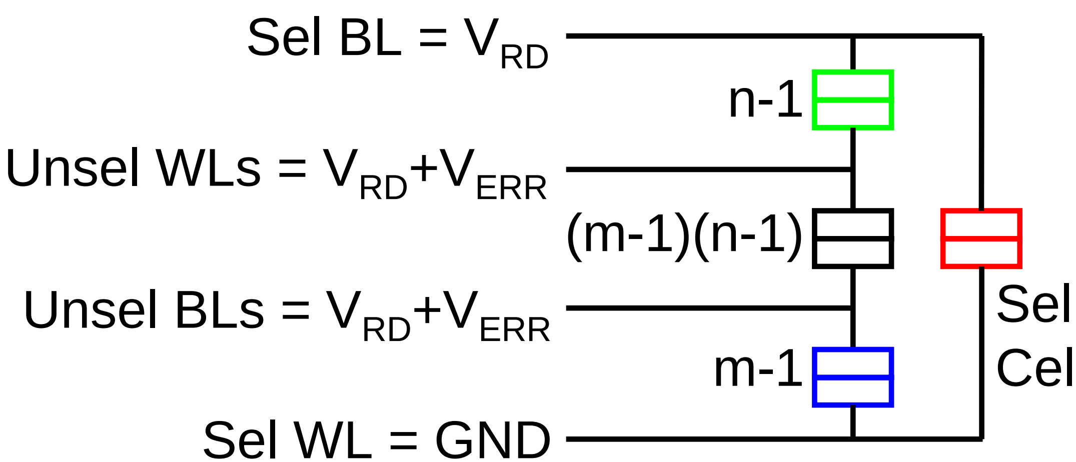


- Unselected BLs, WLs = $V_{WR}/2$
- Selected BL / WL = GND / V_{WR} or V_{WR} / GND
- Selected bit sees +/-V_{WR}, half-selected +/-$V_{WR}/2$
- 2:1 voltage margin - not bad
- Half-selected cell currents ● ● must not create:
  - Large IR drops along selected WL / BL - degrade 2:1 margin
    - R_{MTJ} >> 1.6KΩ for linear IV, 128 b/line, R_{LINE} =0.2Ω/b
  - Excessive write power
    - Could lose power advantage over conventional MRAM
    - $I(V_{WR}/2) = 40\lambda A$, 128b/line ~ conventional MRAM at 5mA
- Non-linear IV may be good for reducing half-selected cell currents

Cross-Point Read

- Selected BL = V_{RD}, selected WL = GND, unselected WLs & BLs = $V_{RD}+V_{ERR}$
- BL half-selected current < signal current
  - V_{ERR} < 0.4mV for linear IV, V_{RD}=250mV, MR=40%, 128b/BL
  - Must use offset-compensating techniques - complex, slow
  - Or use very non-linear device to reduce I(V = +/- a few mV)
- WL half-selected current must not create large IR drop along selected WL
  - R_{MTJ} > 8KΩ for 128b/WL, R_{WL} = 0.2Ω/b , MR = 40% - even slower





Summary

- Spin-switching an attractive candidate for "2nd generation" MRAM
  - Potential advantages in power, write margin, process cost, density
- Simple, fast sensing requires MR > ~ 10%, V_{RD} > ~ 100mV plus margin
- Additional device requirements based on array architecture:
  - 1T1MTJ / 2T1MTJ
    - At read conditions, $R_{MTJ} >> R_{FET}$ (~1KΩ) to avoid effective MR loss
    - Write currents limited by FET to I_{SW} < ~ 0.5mA
    - 2T1MTJ allows more symmetric switching at cost of density
  - Cross-point
    - Half-selected write & read currents create serious problems for:
      - Write margin, write power, read margin

Acknowledgements

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References

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